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Study of the Physico-Structural Properties of Semiconductor Thin-Film Devices

By: BEN OTHMANE Djemâa

Before the jury:

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الجمهوريـــة الجزائريـــة الديمقراطيـــة الشعبيـــة
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Étude des propriétés physico-structurales des composants en couches minces semi-conductrices

Par : BEN OTHMANE Djemâa

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Dedications

To my beloved parents

Whose unwavering love and guidance have shaped me into the person I am today

To my cherished brothers and sisters

Whose bond and support have been a source of strength and joy throughout my life

To my second father Dr. Mohamed Ben Othmane

Who has always supported and guided me throughout my life

To all those who hold a special place in my heart

Your presence and care have enriched my life beyond measure

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-	**President:**	Bouzid HADJOUDJA	Professor	UBM-Annaba
-	**Examiners:**	Brahim BELFARHI	Professssor	U. Guelma
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Lastly, with the deepest gratitude, I extend my heartfelt thanks to **my parents.**Their unwavering belief in me, their sacrifices, and their constant encouragement to pursue my dreams without hesitation have been the driving force behind my determination to complete this work.Thank you for instilling in me the value of knowledge, the strength of patience, and the courage to dream.

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ملخص

تهدف هذه الدراسة إلى تحسين أداء الترانزستورات ذات الأغشية الرقيقة المصنوعة من السيليكون غير المتبلور المهدرج (a-Si:H TFTs)، من خلال تحليل تأثير خصائص العازل البوابي وسمك الطبقة النشطة باستخدام محاكاة برنامج SILVACO ATLAS. تم اعتماد بنية مرجعية تم التحقق من صحتها، حيث طابقت بيانات التيار-الجهد (I-V) التجريبية بدقة بلغت 99%، لدراسة ثلاثة عوامل رئيسية: سُمك العازل البوابي، خصائص المواد العازلة) عالية مقابل منخفضة السماحية(κ – ، وسمك الطبقة النشطة.أظهرت محاكاة تغيير سُمك العازل Si_3N_4 من 300 نانومتر إلى 15 نانومتر تحسنًا ملحوظًا في الأداء الكهربائي للجهاز، حيث تم تسجيل القيم التالية: V_T=4.86 V، μ_{FE}≈0.1 $cm^2/V{\cdot}s$، SS=0.47 V/decade، و C_i=2.21×10⁻⁸ F/cm^2. وقد تبعت الخصائص اتجاهات أُسّية وخطية مع السمك، ونُموذِجت بالعلاقة: $P=P_0+\alpha\exp(\beta\cdot d_i)$، باستثناء SS. تم اختبار مجموعة واسعة من المواد العازلة ذات السماحيات (κ) تتراوح بين 3.9 و300، حيث برزت مادة $SrTiO_3$ كأفضل خيار، محققةً I_{DS}=2.82×10⁻⁵ A؛ C_i=2.65×10⁻⁹ F/cm^2، V_T=3.9 V، μ_{FE}=0.0603 $cm^2/V{\cdot}s$، I_{on}/I_{off}=6.28×10⁷، وSS=0.7691 V/decade.كما أدت تقليصات سمك الطبقة النشطة من 300 نانومتر إلى 15 نانومتر إلى تحسن كبير: تيار تشغيل أعلى) من 5.91×10⁻⁶ إلى 2.97×10⁻⁴(A ، وتيار تسريب أقل) من 1.29×10⁻¹¹ إلى 2×10⁻¹⁸(A ، ونسبة Ion/Ioff مرتفعة، وارتفاع أُسّي في) µFE من 0.10 إلى 14.55(cm²/V·s ، مع انخفاض خطي في VT و.SSأُقترحت بنية محسّنة للترانزستور باستخدام مادة $SrTiO_3$وسماكات طبقات 15 نانومتر، حيث تحققت القيم التالية: V_T = 3.21 V، C_i = 1.77×10⁻⁵ F/cm^2، Ion = 0.609 A، Ioff = 8.28×10⁻²⁰ A، Ion/Ioff = 7.36×10¹⁸، والمجال الكهربائي الأقصى = 9.5×10⁵ V/cm. تُبرز هذه النتائج الإمكانيات الكبيرة لاستخدام العوازل عالية السماحية مع التصميمات الهندسية المُحسّنة لدفع حدود تكنولوجيا الترانزستورات a-Si:H نحو تطبيقات الجيل القادم من الإلكترونيات المرنة، الشفافة، وذات الكفاءة الطاقوية العالية.

الكلمات المفتاحية: ترانزستورات الأغشية الرقيقةa-Si:H ، العازل البوّابي، المواد عالية السماحية(κ) ، سمك الطبقة النشطة، المحاكاة العددية، SILVACO ATLAS، تحسين الأجهزة.

Abstract

This study aims to optimize hydrogenated amorphous silicon thin-film transistors (a-Si:H TFTs) by examining the effects of gate dielectric and active layer parameters through SILVACO ATLAS simulations. A validated reference structure, matching experimental I-V data with 99% accuracy, was used to investigate three critical factors: gate dielectric thickness, dielectric material properties (high-κ vs. low-κ), and active layer thickness. Varying the Si_3N_4 dielectric thickness from 300 nm to 15 nm showed that thinner layers improved device performance, with V_T = 4.86 V, $\mu FE \approx 0.1$ cm²/V·s, SS = 0.47 V/decade, and $C_i = 2.21\times10^{-8}$ F/cm². Parameters followed exponential and linear trends with thickness, modeled as $P = P_0 + \alpha\cdot\exp(\beta\cdot d_i)$, except SS. A range of dielectric materials (κ = 3.9–300) was tested; $SrTiO_3$ emerged as the best, yielding $I_{DS} = 2.82\times10^{-5}$ A, $C_i = 2.65\times10^{-9}$ F/cm², V_T = 3.9 V, μ_{FE} = 0.0603 cm²/V·s, $I_{on}/I_{off} = 6.28\times10^{7}$, and SS = 0.7691 V/decade. Scaling the active layer thickness from 300 nm to 15 nm significantly enhanced performance: higher Ion (5.91×10^{-6} to 2.97×10^{-4} A), lower I_{off} (1.29×10^{-11} to 2×10^{-18} A), higher $I_{on/Ioff}$, and μ_{FE} rising exponentially (0.10 to 14.55 cm²/V·s), with linear drops in V_T and SS. An optimized TFT structure using $SrTiO_3$ and 15 nm thick layers achieved V_T = 3.21 V, $C_i = 1.77\times10^{-5}$ F/cm², I_{on} = 0.609 A, $I_{off} = 8.28\times10^{-20}$ A, $I_{on}/I_{off} = 7.36\times10^{18}$, and peak field = 9.5×10^{5} V/cm. These results underline the promise of high-κ dielectrics and geometric scaling for advanced flexible, transparent, and energy-efficient electronics.

Keywords: *a-Si:H TFT, Gate dielectric, High-κ materials, Active layer thickness, Numerical Simulation, SILVACO ATLAS, Device optimization.*

Résumé

Cette étude vise à optimiser les transistors à couches minces en silicium amorphe hydrogéné (a-Si:H TFT) en analysant, via des simulations SILVACO ATLAS, l'effet des paramètres de la couche diélectrique de grille et de la couche active. Une structure de référence validée, reproduisant les courbes I-V expérimentales avec une précision de 99 %, a permis d'examiner trois facteurs critiques : l'épaisseur du diélectrique de grille, les propriétés des matériaux diélectriques (haute-κ vs basse-κ), et l'épaisseur de la couche active. La variation de l'épaisseur du diélectrique Si_3N_4 de 300 nm à 15 nm a montré que les couches plus fines améliorent les performances : V_T=4,86 V, μ_{FE}≈0,1 cm²/V·s,SS=0,47 V/décade et C_i= 2,21×10⁻⁸ F/cm². Les paramètres suivent des lois exponentielles et linéaires avec l'épaisseur, modélisées par $P=P_0+\alpha exp(\beta \cdot d_i)$, sauf pour SS. Une large gamme de matériaux diélectriques (κ=3,9 à 300) a été testée; $SrTiO_3$ s'est révélé le plus performant avec I_{DS}=2,82×10⁻⁵ A, C_i=2,65×10⁻⁹ F/cm², V_T=3,9 V, μ_{FE}=0,0603 cm²/V·s, I_{on}/I_{off}=6,28×10⁷ et SS=0,7691 V/décade. La réduction de l'épaisseur de la couche active de 300 nm à 15 nm a significativement amélioré les performances : courant "on" plus élevé (de 5,91×10⁻⁶ à 2,97×10⁻⁴ A), courant "off" plus faible (de 1,29×10⁻¹¹ à 2×10⁻¹⁸ A), rapport I_{on}/I_{off} plus élevé, et μ_{FE} passant de 0,10 à 14,55 cm²/V·s, avec une diminution linéaire de V_T et SS. Une structure optimisée intégrant le $SrTiO_3$ avec des couches de 15 nm a permis d'atteindre : V_T=3,21 V, C_i=1,77×10⁻⁵ F/cm², I_{on}=0,609 A, I_{off}=8,28×10⁻²⁰ A, I_{on}/I_{off}=7,36×10¹⁸, et un champ électrique maximal de 9,5×10⁵ V/cm. Ces résultats soulignent le potentiel des diélectriques à haute permittivité et de la réduction géométrique pour les électroniques flexibles, transparentes et économes en énergie de nouvelle génération.

Mots-clés: *a-Si:H TFT, Diélectrique de grille, Matériaux à haute permittivité, épaisseur de la couche active, Simulation numérique, SILVACO ATLAS, Optimisation des dispositifs.*

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List of abbreviations and symbols

Abbreviations	Signification
a-Si:H	Hydrogenated amorphous silicon
BCE	Back-channel etched
BCP	Back-channel passivated
$\boldsymbol{C_{ox}}$	Overall capacitance of the dielectric oxide
C_{OX}	Gate oxide capacitance per unit area
$(C_{ox})_{UA}$	Capacitance per unit area for dielectric oxide
C_{SiO2}	Capacitance of SiO_2
CVD	Chemical vapor deposition
D_n	Diffusion coefficients for electrons
DOS	Density of states
Dp	Diffusion coefficients for holes
E	Eenergy
$\boldsymbol{E}$	Local permittivity
E_c	Conduction band energy
E_F	Spatially independent reference energy known as the Fermi level
E_g	Band gap energy
EGA	Energy corresponding to Gaussian distribution peak for acceptor-like states
EGD	Energy corresponding to Gaussian distribution peak for donor-like states
$\overrightarrow{\boldsymbol{E_n}}$	Electric field acting on electrons
EOT	Equivalent oxide thickness
$\overrightarrow{\boldsymbol{E_p}}$	Electric field acting on holes
Ev	Valence band energy
$f(\varepsilon)$	Probability that an available electron state with energy ε.
g_{GA}	Acceptor-like Gaussian deep level band states
g_{GD}	Donor-like Gaussian deep level band states
G_n	Generation rates for electrons
G_p	Generation rates for holes
gTA	Acceptor-like exponentially decaying conduction band tail states
gTD	Donor-like exponentially decaying valence band tail states
$\boldsymbol{h}$	Planck constant

$i_{a\text{-}si:H}$	Undoped hydrogenated amorphous silicon
I_{on}/I_{off}	I_{on}/I_{off} ratio
j_n	Electron current densities
j_p	Hole current densities
K	Boltzmann's constant
k_{SiO2}	Dielectric constant (relative permittivity) of SiO_2
LCDs	Liquid crystal displays
M	Effective surface mobility of the carriers
$\boldsymbol{m_e^*}$	Effective mass of electrons
$\boldsymbol{m_h^*}$	Effective mass of holes
MISFET	Metal-insulator-semiconductor field-effect transistor
N	Free electron carrier concentrations
$N_{a\text{-}si:H}$	Doped hydrogenated amorphous silicon (Type N)
N_C	Effective density of states for electrons
N_{C300}	Effective density of states in the conduction band at temperature of 300 K
NGA	Maximum density of acceptor-like Gaussian states
NGD	Maximum density of donor-like Gaussian states
$\boldsymbol{n_{ie}}$	Effective intrinsic concentration
N_{TA}	Density of acceptor-like tail states at the conduction band edge
N_{TD}	Density of donor-like tail states at the valence band edge
N_V	Effective density of states for holes
N_{V300}	Effective density of states in the valence band at temperature of 300 K
P	Free hole carrier concentrations
$P_{a\text{-}si:H}$	Doped hydrogenated amorphous silicon (Type P)
PECVD	Plasma-Enhanced Chemical Vapor Deposition
Q	Electron charge
R_n	Recombination rates for electrons
R_p	Recombination rates for holes
SILVACO	Silicon Valley Corporation
SS	Subthreshold swing
T	Temperature
TCAD	Technology Computer-Aided Design
TFT	Thin-Film Transistor
$T_{high\text{-}\kappa\text{-}ox}$	High-k dielectrics (oxide) thickness
T_L	Lattice temperature
T_{SiO2}	Thickness of SiO_2
V_{DS}	Source-to-drain voltage
V_{eff}	Effective gate voltage
V_{GS}	Gate-to-source voltages
V_T	Threshold Voltage
W	Effective gate mask width

W_{GA}	Characteristic decay energy for the Gaussian distribution of acceptor-like states.
W_{GD}	Characteristic decay energy for Gaussian distribution peak of donor-like states.
W_{TA}	Characteristic decay energy for the tail distribution of acceptor-like states
W_{TD}	Characteristic decay energy for the tail distribution of donor-like states
μ_{FE}	Field-Effect Mobility
μ_n	Electron mobilities
μ_p	Hole mobilities
E	Energy level of a specific electronic state
ε_0	Permittivity of free space (vacuum permittivity)
ε_{SiO2}	Permittivity (absolute) of SiO_2
Ψ	Electrostatic potential
$\boldsymbol{\nabla n}$	Gradient of electron concentration
$\boldsymbol{\nabla p}$	Gradient of holes concentration
2D	Two-Dimensional
3D	Three-Dimensional

General introduction

Hydrogenated amorphous silicon (a-Si:H) remains a material of great significance in the domain of thin-film electronics [1,2]. Due to its low production cost, good uniformity over large areas, and relatively simple fabrication processes, a-Si:H has found widespread use in thin-film transistor (TFT) technology, particularly in active-matrix liquid crystal displays (AMLCDs), image sensors, and emerging flexible electronics [3-8]. Despite the development of alternative materials such as organic semiconductors, metal oxide semiconductors, and low-temperature polysilicon, a-Si:H TFTs continue to play a major role, especially in applications requiring cost-effective and scalable manufacturing [3]. Nevertheless, the inherent limitations of a-Si:H TFTs including relatively low carrier mobility, threshold voltage instability, and poor subthreshold behavior have motivated ongoing research efforts to optimize their performance [9].

Simulation based on physical phenomena has become essential for designing Thin-Film Transistors (TFTs) due to its speed, cost-effectiveness, and ability to provide insights that are difficult or impossible to measure directly [10]. In this work, we used the SILVACO software, specifically the ATLAS simulator, which is ideal for semiconductor device simulation [11]. ATLAS allows both 2D and 3D modeling of TFT structures, predicting electrical behavior under AC, DC, and transient conditions [10]. This helps in understanding the physical mechanisms of TFT operation and optimizing their performance. We applied this tool to simulate and enhance the a-Si:H TFT structures in our study.

This research work concerns an extensive investigation and optimization of a-Si:H TFTs through simulation techniques, with the objective of performance improvements. Hence, this

thesis combines materials science insights, advanced simulation techniques, and device engineering to address critical challenges in a-Si:H TFT technology.

This thesis is structured into three chapters: a fundamental study of a-Si:H material and TFT operation principles, a detailed exploration of the simulation methods using SILVACO software, and a comprehensive simulation-based analysis and optimization of device structures.

The first chapter provides an essential overview of hydrogenated amorphous silicon, offering critical insights into its structural and electronic properties. It establishes a detailed understanding of the material, focusing on its atomic arrangement, the incorporation of hydrogen, and how these factors influence its performance as a semiconductor. The chapter further investigates the density of states (DOS) and the unique electrical characteristics of a-Si:H, which are crucial for its application in thin-film transistor technology.

The principles of transistor operation are also reviewed, tracing the historical development of TFTs from early foundations to present-day configurations. Different structural designs, including top-gate, bottom-gate, bi-layer (back-channel etched, BCE), and tri-layer (back-channel passivated, BCP) TFTs, are presented and compared. This section also defines the electrical characteristics and main performance parameters essential for evaluating TFT operation, such as threshold voltage, field-effect mobility, subthreshold swing, and on/off current ratios. Particular attention is paid to the dielectric material selection, distinguishing between low-κ and high-κ dielectrics, and explaining their influence on gate control and device stability.

The second chapter, focuses on device simulation methodologies. Thus, the SILVACO TCAD environment is introduced, with a particular emphasis on the ATLAS simulator. The modules ATHENA, DeckBuild, DEVEDIT, and TonyPlot are also described, highlighting their roles in device design, mesh creation, structure definition, and results analysis. Fundamental semiconductor physics governing the simulation, including Poisson's equation, carrier continuity equations, transport equations, and models like drift-diffusion

and energy balance transport, are elaborated to ensure a clear understanding of the simulation foundations. Carrier statistics, material property modeling, and defect state incorporation specific to amorphous semiconductors are discussed to accurately represent the behavior of a-Si:H TFTs in simulations.

The third and most chapter concerns the presentation of the obtained results, their analysis, their quantification and their validation. The work begins by establishing a reference a-Si:H TFT structure based on experimental designs putting into evidence the validation of simulation models through the comparison of current-voltage characteristics and extracted electrical parameters. Then, to optimise the a-Si:H TFTs performances we investigated three main parameters: (i) the gate dielectric thickness, (ii) the dielectric constant (κ), and (iii) the active layer thickness. To do so, we first chose the scaling down film thicknesses from 300 to 15 nm for both dielctric and active layers then we considered a great number of dielectric materials: $SrTiO_3$, $BaSrTiO_3$,$SrZrO_3$, Nb_2O_5, TiO_2, HfO_2, Ta_2O_5, La_2O_5, CeO_2, ZrO_2, Gd_2O_5, Y_2O_3, Al_2O_3, Si_3N_4, and SiO_2.

Moreover, in each of these parametric studies, the key performance indicators (Threshold voltage, Capacitance per unit area, Field-effect mobility, Subthreshold swing, and *Ion/Ioff* ratio) are carefully quantified. This quantification is carried out through detailed curve fitting of the simulated results, enabling the extraction of empirical equations that describe the variation of each parameter as a function of the thickness of gate dielectric and atcive layers as well as the dielectric constants.

Finally the general conclusion regroups the most important obtained results and their analysis which led to the proposition of optimised a-Si:H TFT as part of practical design strategies to improve device performance, contributing to the advancement of cost-effective and scalable thin-film electronics.

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CHAPTER I:

Hydrogenated amorphous silicon thin-film transistors

I.1 INTRODUCTION

Hydrogenated amorphous silicon, a unique form of silicon with a disordered atomic structure, exhibits a range of intriguing properties and has emerged as a prominent material for various electronic devices. Therefore, This chapter deals with the attractive world of hydrogenated amorphous silicon and its applications in thin-film transistor technology. To better understantd the behavior and potential applications of a-Si:H-based TFTs, we start this review with an overview of the fundamental characteristics and properties of a-Si:H, highlighting its amorphous nature, hydrogen incorporation, and density of states.Then, the fundamental working principles and operational mechanisms of a-Si:H TFTs are examined in detail: device physics, electrical characteristics, and performance parameters. Finally, to study the permittivity, ε_r, effects of these TFT deivices , we recall several dielectric materials that have attracted great attention for their versatile applications in modern industries. These materials, with high and low dielctris constant, κ, play a very important role in the TFT perfomrances.

I.2 HYDROGENATED AMORPHOUS SILICON

I.2.1 Atomic structure

Silicon, due to its abundance and unique semiconductor properties, is currently the most favored material for electronic devices. It is extensively utilized in the computer industry, flat-panel displays, and solar-cell applications, primarily for the production of transistors and integrated circuits. Silicon is found in three different forms:

- *Monocrystalline or single-crystal silicon*: Possesses an infinitally uninterrupted atomic structure in the crystal lattice
- *Polycrystalline silicon*: Consists of multiple small silicon crystals interconnected by grain boundaries.
- *Amorphous silicon*: In contrast, lacks a crystalline periodic structure; it lacks long-range order bur conserves short-range coordination bonds.

The amorphous silicon atomic structure, charactrised by a toplogical disorder, most of the Si atoms are four-fold coordinated, similar to that of cystalline silicon (Figure I.1). It also contains sevral dangling bounds. Frotunately, the presence of hydrogen atoms within the amorphous lattice during its praparations acts as a passivating element that leads to the redictions of the density of defects in the structure [1, 2].

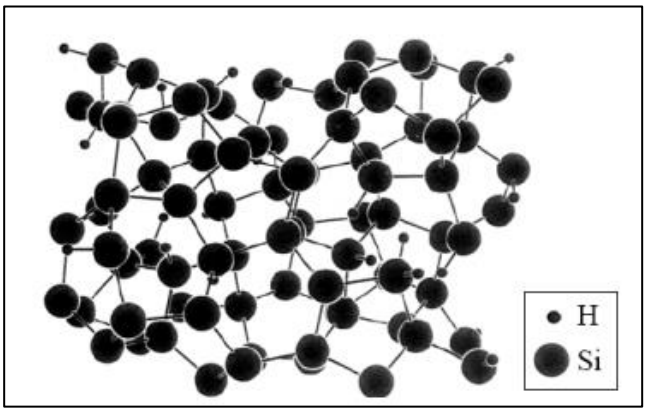

Figure I.1. *Atomic structure of hydrogenated amorphous silicon [2].*

Although amorphous silicon does not possess an ordinary crystal lattice, it conserves a short rage odrer that ex tends over a few interatomic distances. Therefors, a-Si solidifies with a covalent bond strcuture. The values of covalent bonding angless and length of silicon atoms are quite similar for crystalline and amorphous Si with a small difference of about respectively. This hort range order leads to bery important effects on the electrical and optical characteristics of amorphous silicon. The distortion in bond lengths and bond angles leads to a broadened distribution of states, resulting in carrier localization and strong carrier scattering. These effects subsequently reduce the effective mobility of carriers. The dangling bounds give rise to electronic defect states that occupy deep states in the misdddle of the a-Si energy gap. within the middle of the amorphous silicon band gap [2]. The determination of the atomic structure of amorphous materials could be achieved via seneral experimental methods in particular diffraction techniques: X-ray, electron, neutron, and EXAFS (extended X-ray absorption fine structure). These techniques give valuable informations about the structural properties as well as their behavior [3-7].

I.2.2 Hydrogen in amorphous silicon

The incorporation of hydrogen into amorphous silicon during its el bration by physcial vapour deposition leads (i) to the saturation of defects which consists mainly of dandling bounds, (ii) to the couteracting of the inherent over-coordination by forming silicon-hydrogen bonds [8] and to optimise perfomrances of a-Si performances [8, 9].. Furthermore, it is experimentally shown that hydrogen can exist in a-Si:H in various topological "H microstructure" configurations for which available states are filled up to the hydrogen chemical potential.-This leads to a wide range of phenomena related to hydrogen redistribution and transport in the material [9].

I.2.3 a-Si:H Density of states

The a-Si:H electronic and optical properties are greatly influenced by the density of states (DOS) within the band gap [3], which is typically around 1.8 eV [10]. The DOS affects different parameters of the amorphous semicondcutos, such as: mobility (μ), optical absorption (α), and emission characteristics. The good control of the DOS via the arrangement of Si and H_2 atoms, as well as their bonding configurations, makes it possible to master the electronic behavior of a-Si:H-for various thin-film applications such as: solar cells, transistors, and other electronic devices [10].

Thus, the determination of the density of stanes of a-Si:H is of a major challenge for optimised electronic properties in odrer to design anf fabricate devices for specific applications. There exist several techniques to determine a-Si:H density of states that can be classified into three main categories [3, 11-16]:

(i) ***Electron-spin resonance (ESR):*** This technique is used to accurately deduce the defect density in undoped a-Si and to gove good information about the presence and characteristics of defects in the material [12].

(ii) ***Optical defect spectroscopy:*** This group of methods include: photoacoustic spectroscopy (PAS), photocurrent spectroscopy (PCS), and photothermal deflection spectroscopy (PDS) [3].

(iii) ***Space charge spectroscopy:*** This group of methods include: space charge limited current (SCLC) measurements [13], field-effect (FE) measurements [14], and deep-level transient spectroscopy (DLTS) [15,16]. The first used technique used to determine the density of states distribution in a-Si was the Field-effect measurement [3].

Figure I.2.a show the density of states of disordered materials and Figure I.2.b show the density of states of undoped a-si:H (i a-si:H) and doped a-si:H (N and P a-si:H). The density of states in a-Si:H, is often characterized by four distinct regions:

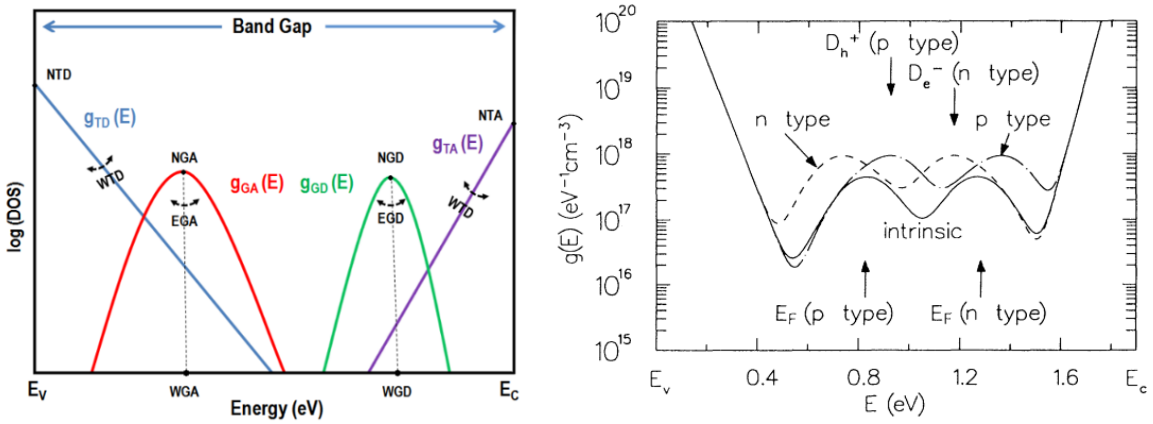

Figure I.2. *Schematic electronic structure (a) disordered materials density of states [16], and (b) Undoped and doped a-si:H density of states [17].*

- ✓ ***Acceptor-like exponentially decaying conduction band tail states [$g_{TA}(E)$]:*** These states follw an exponential decay with energy; they are *(i)* like acceptor states, (ii) located in the conduction band tail and (iii) associated with localized electronic states that extend into the band gap.
- ✓ ***Donor-like exponentially decaying valence band tail states [$g_{TD}(E)$]:*** These states exhibits an exponential decay with energy; they are (i) like donor states, (ii) are positioned in the valence band tail, and (iii) associated with localized electronic states that extend into the band gap..
- ✓ ***Acceptor-like Gaussian deep level band states [$g_{GA}(E)$]:*** These states are characterised by a : (i) deep location within the band gap, (ii) Gaussian-shaped density distribution,

(iii) acceptor-like beahviour donar-like beahviour with the highest density near and low towards band edges.

The presence and distribution of these states afffects the carrier transport, recombination processes, and overall device performance in a-Si:H-based devices. The density of states can be modeled as:

$$g(E) = g_{TA}(E) + g_{TD}(E) + g_{GA}(E) + g_{GD}(E) \quad \text{(I. 1)}$$

with:

$$g_{TA}(E) = N_{TA} exp\left[\frac{E-E_c}{W_{TA}}\right] \quad \text{(I. 2)}$$

$$g_{TD}(E) = N_{TD} exp\left[\frac{E_F-E}{W_{TD}}\right] \quad \text{(I. 3)}$$

$$g_{GA}(E) = N_{GA} exp\left[-\left[\frac{E_{GA}-E}{W_{GA}}\right]^2\right] \quad \text{(I. 4)}$$

$$g_{GD}(E) = N_{GD} exp\left[-\left[\frac{E-E_{GD}}{W_{GD}}\right]^2\right] \quad \text{(I. 5)}$$

I.3 THIN-FILM TRANSISTORS

I.3.1 History

A transistor is a key device in-modern microelectronics with many functions, mainly the amplification, the swiching of electrical signals in various circuits, the flow regulation of the electrical currents based on a set of input signals [18] . The active layers of such devices are consist of semicondcutors such as silicon or gallium arsenide. The milestone invention of the transistor, in 1947 by Bardeen, Brattain and Shockley, transformed the electronics era facilitated the miniaturization of circuits and created integrated circuits (ICs), which today's digital devices [19].

Transistors can be classified into two types (Table I.1): (i) Bipolar Junction Transistors (BJT) which are governed by currents with both charge carriers (elctrons and holes) and (ii) Field-Effect Transistors (FET) whose operations are based on voltages. These devices are integrated in many analog and digital electronic products:–computers, smartphones, amplifiers, power supplies, and communication systems [19, 20].

Table I.1. *Categories of transistors based on their operational principles [20].*

Category of transistor	Operation Principle	Applications
Bipolar Junction Transistor (BJT)	Current-controlled, small base current controls larger current between collector and emitter.	Amplifiers, switches, motor control, analog circuits.
Field-Effect Transistor (FET)	Voltage-controlled, reverse-biased p-n junction controls current flow between source and drain.	Low-noise amplifiers, analog circuits.

The principle of the field-effect transistor [21-25] was first proposed by Lilienfeld in 1930. However, it wasn't until 1959 that Kahng and Atalla produced the first silicon-based metal-oxide-semiconductor FET (MOSFET). In 1962, Weimer et al. introduced the concept of thin-film transistors based on FET principles, and in the same year, they successfully developed transistors using polycrystalline inorganic semiconductorsleading to the development of the first organic thin-film transistors (OTFTs) in 1980. The different types of Field-Effect Transistors are regrouped in (Table I.2) [25]. Figure I.3 shows the historical developments of TFT technology [26-28].

Table I.2. *Different types of Field-Effect Transistors (FETs)[25].*

Type of FET	Description
JFET (Junction FET)	Voltage-controlled transistor with a pn-junction gate.
MOSFET (Metal-Oxide-Semiconductor FET)	Most commonly used FET, with an insulated gate for high input impedance.
HEMT (High Electron Mobility Transistor)	Specialized FET using heterojunctions for high-speed and high-frequency applications.
TFT (Thin-Film Transistor)	A type of FET built on an insulating substrate, used in displays and flexible electronics.
FinFET (Fin Field-Effect Transistor)	Advanced 3D MOSFET design for better control and efficiency in nanoelectronics.

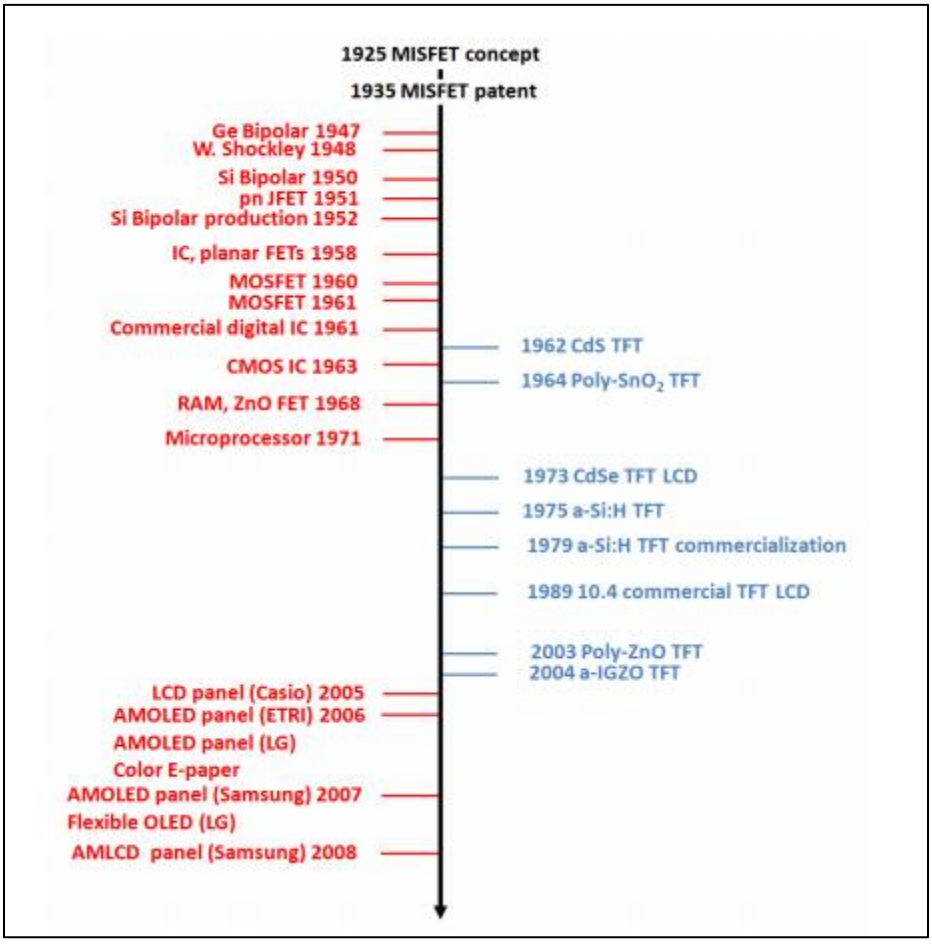

Figure I.3. *History of oxide thin - film transistors [26-28].*

I.3.2 TFTs structures

A thin-film transistor is a particular type of field-effect transistor that consists of an ensemble of layers deposited on a substrate. These layers include (i) semiconducting active layers, (ii) gate dielectric layer (insulator), and (iii) metallic contacts (gate, source, and drain). The active layer in a-Si TFTs is intrinsic a-Si, while silicon nitride is commonly used as the gate dielectric (SiNx) [3].

The arrangement of the relative position of the source/drain and gate electrodes with respect to the semiconductor active layer is the key parameter for the classification of TFT. They could be staggered or coplanar structures with top or bottom gates, as illlustrated in Figure I.4. Thus, the basic TFT structures can be classified into four categories [27-32]: Staggered Bottom gate, Staggered Top gate, Coplanar Bottom gate, and Coplanar Top gate. All these configuations allow the the current flow amplification between the drain and the source (I_{DS}) by varying the potential between the gate and the source (V_{GS}). This operation favors the the free charge buildup at the dielectric/semiconductor interface.

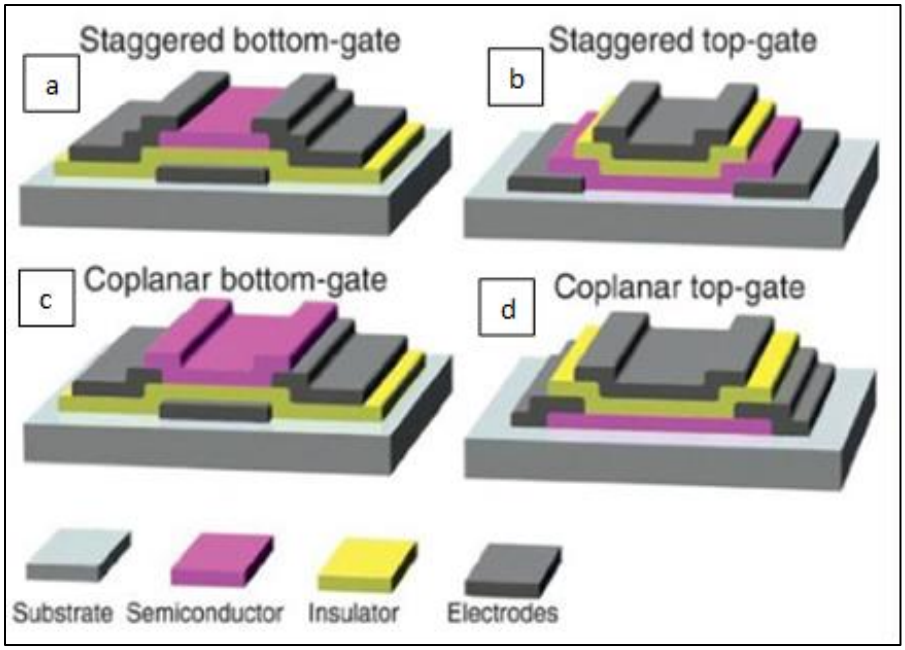

Figure I.4. *Schematics representation of TFT configurations:(a) staggered bottom gate (b) staggered top gate (c) coplanar bottom gate, and (d) coplanar top gate [17].*

I.3.2.1 Top-gate structure

In top gate structure of a thin-film transistor, the gate is situated above the semiconductor layer. Two configrations (staggered or coplanar top gate) are possible in this case.

(i) Figure I.4(b) illlstrates the staggered top gate configuration: the gate is located on the opposite sides of the active layer from the drain and source,

(ii) (Figure I.4 (d) shows the coplanar top gate configartaion: all electrodes (gate, source and drain) are positioned on the same side of the active semiconductor.

I.3.2.2 Bottom-gate structure

For the bottom gate TFT structure, the gate is located below the semiconductor active layer. Two configrations (staggered or coplanar top gate) are also possible in this case. When gate electrode is positioned on the opposite side of the semiconductor from the drain and source contacts, the configuration is said to be staggered bottom gate (Figure 1.4.a). For the coplanar bottom gate configuration (Figure 1.4.c) all electrodes (gate, source and drain) are positioned on the same side of the active semiconductor.

The bottom gate structure (known as inverted-staggered structure) that can simply manufactured gives higher electrical performances and have simple manufacturing procedures [3]. The active a-Si layer is placed on top of the gate SiNx dielectric layer in inverted (bottom-gate) a-Si TFT structures.

It is reported that interfaces with a-Si on top of SiNx are better than those with SiNx on top of a-Si since they have a lower interface charge density and hydrogen concentration [30,33,34]. Therefore, the performances of bottom gate a-Si TFTs are more advatageous as far as field-effect mobility, threshold voltages, and subthreshold slopes are concerned.

I.3.2.3 Bi- and Tri-layer back-channel structure

There are two categories of TFTs with an inverted-staggered structure (bottom-gate Structures): bilayer (with a back-channel etched or sliced) and trilayer (back-channel passivated) [3,35]. Figure I.5.a shows a schematic cross-section of two common a-Si:H TFT structures with back channels etched (BCE), and Figure I.5.b shows a schematic cross-section of two common a-Si:H TFT structures back channels passivated (BCP).

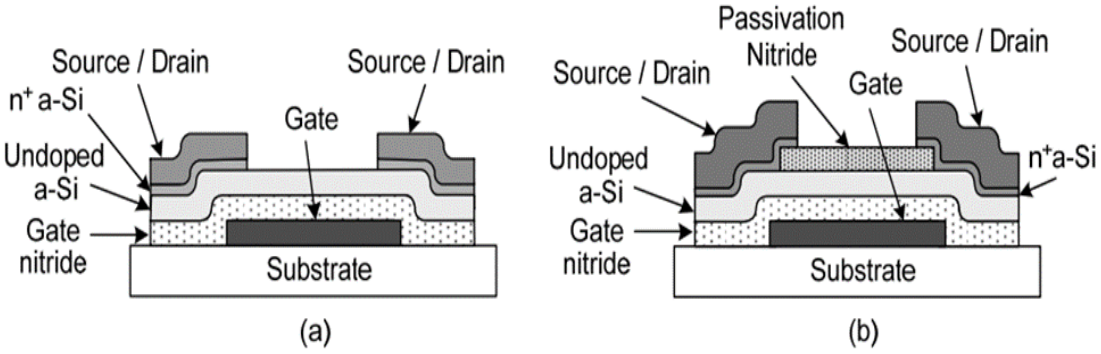

Figure I.5. *Standard a-Si:H TFT structures with a schematic cross-section (a) back-channel etched, and (b) back-channel passivated [35]*

The sequences of the the fabrication process of the bi-layer (BCE) structure (Figure I.5.a) consists of : the depositions depositing the gate SiNx, intrinsic a-Si, and doped n+ a-Si sequentially while maintaining a vacuum environment. the TFT channel length is determined by the separation between the source and drain contacts [35]. The tri-layer (BCP) structure incorporates an additional layer of SiNx on top of the active a-Si layer [3].

I.3.3 TFTs Operation

The operation of the transistors is based on the control of the current circulating between the source and the drain by applying a variable voltage on the gate. It can be operated in the ON or OFF regime. In the ON regime, when the applied voltage is positive, there is accumulation of load at the insulating-semiconductor interface and as soon as it becomes greater than a threshold voltage (V_T), a conductor channel is created thus making it possible

to pass current between the source and the drain when the latter are polarized. In rhe OFF regime, a negative bias of the gate causes a region of low free electron density in the channel [36, 37]. To axplain the a-Si:H TFT operation we use in Figure I. 6 an energy band diagram (a) under a positive gate bias and (b) a schematic representation of density of states distribution.

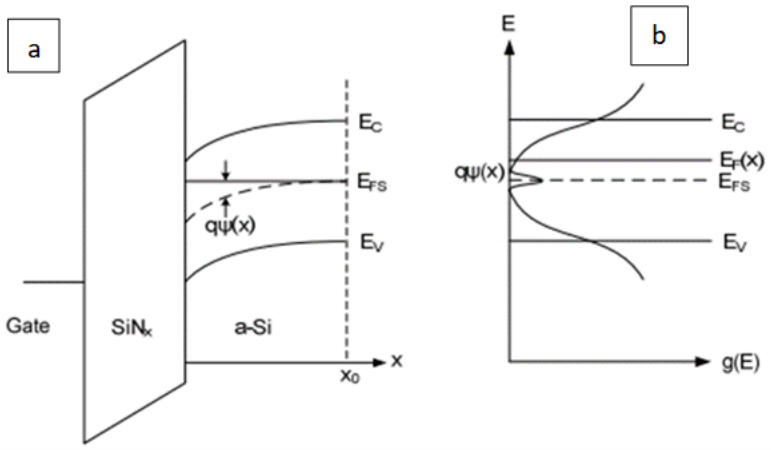

Figure I.6. (a) *Band diagram of an a-Si TFT under positive gate bias, and* (b) *Density of states distribution [3]*

I.3.4 TFT characteristics and performance parameters

I.3.4.1 Electrical characteristics

The electrical characteristics of a-Si:H field effect transistors consist of the determination of (a) the transfer characteristics and (ii) the output characteritiscs. The the transfer characteristics are obtained by plotting drain current-gate voltage (I_D-V_G) as a fuction of drain voltages (V_D). The output characteristics are represented by the drain current-drain voltage verus gate voltages (V_G). Typical

experimental results are illustrated in Figure I.7, obtained for a high-performance a-Si TFT with 150 µm channel width and 15 µm channel length.

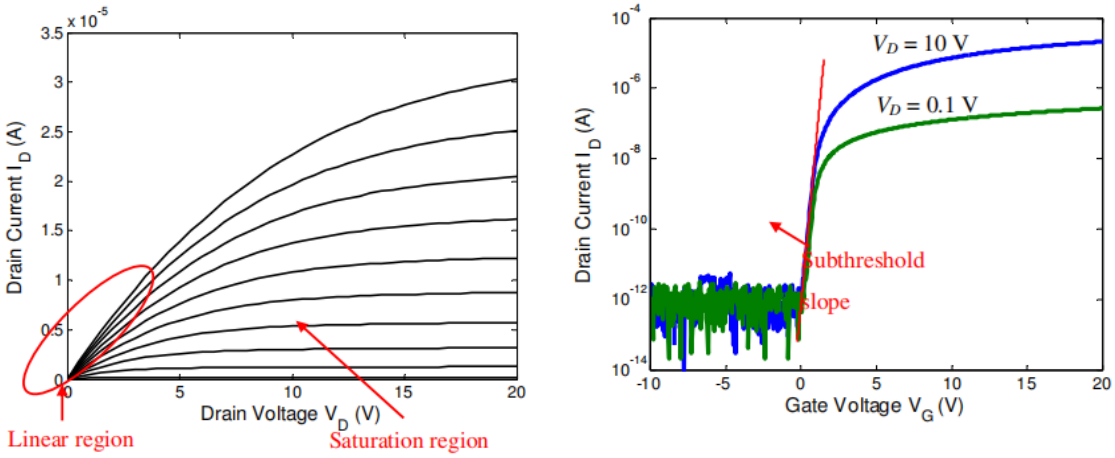

Figure I.7. *I-V characteristics: (a) Output characteristics, and (b) Transfer characteristics of a typical a-Si TFT [42].*

The current-volatge characteristics of thin film transistors can be categorized into three distinct operating modes [32]:

- cut-off mode when $V_{GS} < V_T$,
- linear mode when $0 < V_{DS} < V_{eff}$
- and saturation mode when $V_{eff} < V_{DS}$.

whereV_{DS} is the drain-to-source voltage and V_{eff} is the effective gate voltage, equal to the different between the gate to source voltage V_{GS} and the transistor threshold voltage V_T, $V_{eff} = V_{GS} - V_T$.

I.3.4.2 Main performance parameters

The output characteristics as well as the transfer characteristics can be used to extract several TFT parameters such as: Threshold Voltage, Field-Effect Mobility, Subthreshold swing, I_{on}/I_{off} ratio, Capacitance, Equivalent oxide thicknesses, Electrical resistivity. The main parameters, studied in this thesis, are difined below.

a)Threshold Voltage

The threshold voltage (V_T) is dfined, from the transfer characteristic, as the gate voltage at which substantial drain current initiates its flow [38]. Physically, it corresponds to the minimum gate voltage that propels the channel into a state of strong charge inversion. The threshold voltage can be extracted from the measured transfer characteristics of a-Si:H in several ways such as:

- *Constant Current (CC) method*, which defines V_T as the gate voltage corresponding to a certain predefined practical constant drain current [38-41].
- *Match-Point (MP) method*, which defines V_T as the gate voltage at a pre-established deviation percentage of the drain current from its extrapolated weak inversion conduction behavior [38-42].
- *Linear Extrapolation (LE) method*, which defines V_T as the gate voltage axis intercept of the tangent of the I_{DS}–V_{GS} characteristics at its maximum first derivative (slope) point [38-41].
- *Second Derivative (SD) method*, which defines V_T as the gate voltage at the maximum of the second derivative of the I_{DS}–V_{GS} characteristics,
- *Third-derivative (TD) method* , which defines V_T as the gate voltage at the maximum of the third derivative of the I_{DS}–V_{GS} characteristics, in contradiction to the SD method,
- *Current-to-square-root-of-the-Transconductance Ratio (CsrTR) method*, which defines V_T as the gate voltage axis intercept of the ratio of the drain current to the square root of the transconductance,
- *Transition method* which defines V_T at the transition between weak and strong conduction behaviors, inspired on the integral difference function D,
- *Normalized Mutual Integral Difference Method (NMID),* also an integration-based method following the ideas of the previous one,
- *Normalized Reciprocal H function (NRH) method*, which is an improvement to the NMID method; and
- *Transconductance-to-Current-Ratio (TCR) and its integration -based counterpart the Reciprocal H function (RH) method* .

The Linear Extrapolation (LE) method was applied to determine V_T. In the linear region, this method involves identifying the gate voltage axis intercept (where I_{DS} = 0) of the $I_{DS} - V_{GS}$ curve's linear extrapolation at its peak first derivative point. The V_T value is often computed by subtracting half of the drain-to-source voltage (V_{DS}/2) from this resulting gate voltage axis intercept. For the saturation region, the LE approach is akin to that in the linear region, but it employs the $I_{DS}{}^{1/2} - V_{GS}$ characteristics instead. However, in this study, these characteristics were not considered due to their role as filler in the context of saturation analysis [38]. The threshold voltage (V_T) of TFTs demonstrates variation based on either the capacitance of the gate insulator or the thickness of the semiconductor film. Devices with shorter channel lengths and thicker films tend to exhibit lower threshold voltages. This characteristic is advantageous for low-power applications, broadening the scope for employing TFTs in various contexts [43].

b) Field-Effect Mobility

Field effect mobility (μ_{FE}), a key paramter for device applications, is often employed to describe the electrical behavior of the channel. It is defined as [41]:

$$\mu_{FE} = \frac{L_g}{W\, C_{ox}\, V_{DS}} \left(\frac{\partial I_{DS}}{\partial V_{GS}}\right) \qquad \text{(I.1)}$$

where C_{ox} represents the gate insulator capacitance per unit area, while Lg and W denote the channel length and width, respectively.

c) Subthreshold swing

The subthreshold swing (SS) value is defined as the alteration in V_{GS} (gate-to-source voltage) necessary to produce a tenfold change in current below the threshold level [44].. The values imporatnce of subthreshold swing lies in its ability to dictate the minimal V_{GS} needed to transition a TFT from the off state [45]. SS represents the reciprocal of the steepest slope in the semi-logarithmic plot of the transfer characteristic; it can be calculated using the following equation [46-48]:

$$SS = [\frac{\partial V_{GS}}{\partial \log(I_{DS})}]_{max} \quad \text{(I.2)}$$

d) I_{on}/I_{off} ratio

The parameter I_{on}/I_{off} characterizes the magnitude of the difference between the on-state current and off-state current in the transfer characteristic when plotted semi-logarithmically [49]. This parameter represents the ratio of the current in the accumulation mode to the current in the depletion mode [44]. The on-state current I_{on} represents the maximum I_{DS} within the transfer characteristic's semilogarithmic plot, while the off-state current I_{on}/I_{off} desribes the minimum I_{DS} within the same plot.

e) Capacitance

The expression of the overall capacitance of the dielectric oxide (C_{OX}) is given by [47,50]:

$$C_{ox} = C_{SiO2} = \frac{\varepsilon_0.K_{ox}.L.W}{T_{SiO2}} = \frac{\varepsilon_{Si02}.L.W}{T_{SiO2}} = \frac{\varepsilon_{Si02}.A}{T_{SiO2}} = \frac{\varepsilon_{Si02}.L.W}{T_{SiO2}} = \frac{\varepsilon_{Si02}.A}{T_{SiO2}} = (C_{ox})_{UA}.A \quad \text{(I.3)}$$

where C_{SiO2} stands for the capacitance of $_{SiO2}$, ε_0 denotes the permittivity of free space (also known as vacuum permittivity), κ_{SiO2} is the dielectric constant (relative permittivity) of SiO_2, ε_{SiO2} represents the permittivity (absolute) of SiO_2, T_{SiO2} is the thickness of SiO_2, L and W correspond to the length and width of the dielectric oxide (or plates), A stands for the cross-sectional area of the dielectric oxide (or plates), and $(Cox)_{UA}$ represents the capacitance per unit area for the dielectric oxide. This capacitance per unit area is given by the equation:

$$(C_{ox})_{UA} = C_i = \frac{\varepsilon_0 K_{ox}}{T_{ox}} \quad \text{(I.4)}$$

f) Equivalent oxide thicknesses

The equivalent oxide thickness (EOT) of a high-κ dielectric can be formulated as:

$$\mathbf{EOT} = \frac{\mathbf{K_{SiO2}}}{\mathbf{high\text{-}k}} . \mathbf{T_{high\text{-}k\text{-}ox}} \quad \text{(I.5)}$$

where k_{SiO2} is the dielectric constant (relative permittivity) of SiO_2, high-κ represents the relative permittivity of high-κ dielectrics, and $T_{high\text{-}k\text{-}ox}$ is the thickness of the high-κ dielectric (oxide) layer [47,50,51].

g) Electrical resistivity

The electrical resistivity values of the active layers of the a-Si:H TFT devices are determined from the drain current-drain voltage ($I_{DS} - V_{DS}$) characteristics using the following equation [54]:

$$\boldsymbol{\rho} = \frac{\mathbf{v}}{\mathbf{I}} . \frac{\mathbf{W}}{\mathbf{L}} . \mathbf{T} \quad \text{(I.6)}$$

Where *V* stands for the input voltage and *I* represents the output current. Furthermore, *W* and *L* symbolize the width and length of the electrode, respectively, while *T* signifies the thickness of the a-Si:H active layer.

I.4 DIELECTRIC MATERIALS

Dielectric materials belong to the category of electric insulators capable of polarization in response to an external electric field [52-57]. They are classified into two groups: low- κ and high- κ dielectric materials. Dielectric materials have garnered attention for their versatile applications in industries, including linear dielectrics, ferroelectrics, piezoelectrics, pyroelectrics, and multiferroics. The dielectric constant (κ) also known as relative permittivity (ε_r), represents the ratio of the permittivity of a substance to the permittivity of free space. The dielectric constant serves as a parameter that defines a material's capacity to store the electric charge.

I.4.1 Low-κ dielectric materials

Low-κ materials, which are characterised by a-low dielectric constant are substances with a relatively limited capacity to conduct or propagate electric fields or signals. This category (Figure I.8) includes Si-containing materials, particularly those with Si-O bonds, as well as non-Si-containing materials [53, 59].

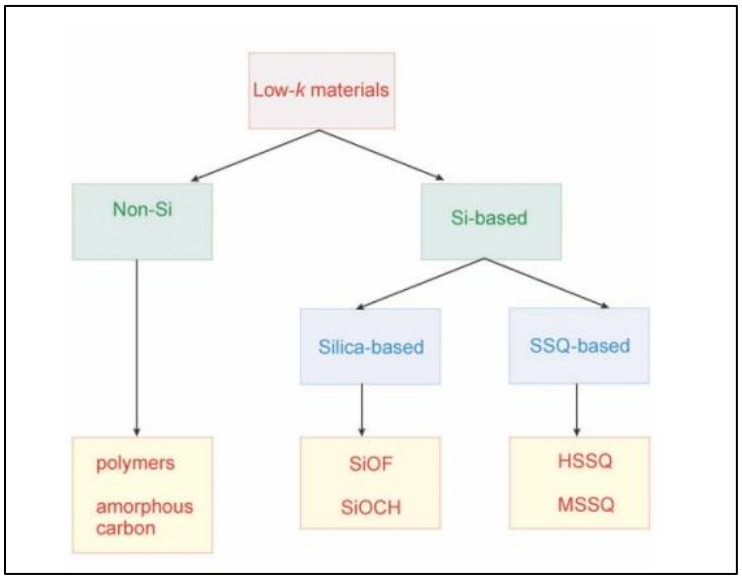

Figure I.8. *A simplified classification scheme of low-k dielectrics [59].*

Si-containing materials can be subdivided into two distinct subgroups: silica-based and silsesquioxane (SSQ)-based materials. The primary distinction between these two groups is rooted in the structural composition of their fundamental units [52]. Silica is identified by its tetrahedral elementary unit (as shown in Figure I.9). To decrease its κ value, specific oxygen atoms can be replaced with elements such as F, C, or CH_3. The incorporation of CH_3 not only results in less polar bonds but also generates additional free space. These silicon oxycarbides (SiOCH) showcase inherent porosity. In the realm of integrated circuit (IC) fabrication, the earliest low-k materials predominantly belonged to the silica-based category, particularly F- or C-doped SiO_2. This preference stemmed from the well-established comprehension of SiO_2 [52].

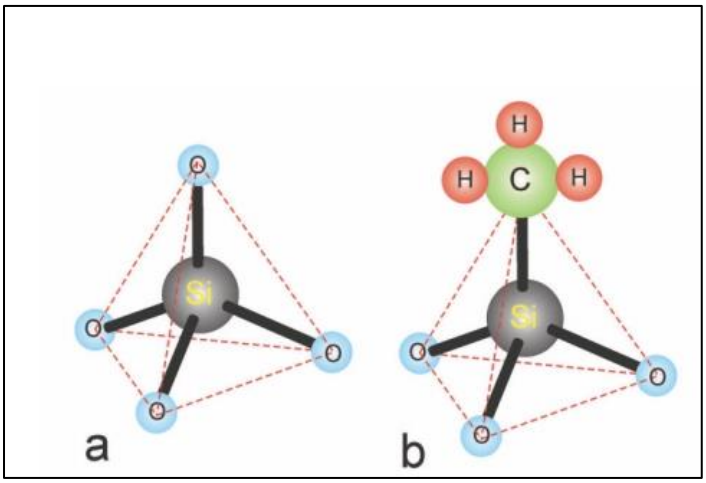

Figure I.9. *A schematic representation (not to scale) of (a) tetrahedral silica unit and (b) the same unit of SiOCH material [52].*

The elementary unit of SSQ consists of Si and O atoms arranged in a cubic structure (Figure I.10). This arrangement creates vacant space at the center of the cube, reducing the material's density and consequently lowering its k value. The cubes can be linked through oxygen atoms, with hydrogen terminating some cube corners, resulting in hydrogenSSQ (HSSQ) materials. In the presence of methyl groups, the cubes can be connected by -CH_2- and terminated with CH_3, forming methyl-SSQ (MSSQ). SSQ cubes are metastable and can degrade into silica tetrahedra, particularly at high temperatures. Consequently, SSQ-based materials represent a combination of SSQ cubes and silica tetrahedra. Both silica- and SSQ-based materials typically exhibit k values ranging from three to four, which can be further reduced through the introduction of porosity [52].

Non-Si based materials primarily consist of organic polymers, offering the advantage of low polarizability, which can results k values as low as two without the need for porosity. However, polymers face a significant drawback in terms of their limited compatibility with current semiconductor processing methods, including low thermal and mechanical stability. While other low-k materials like amorphous carbon and zeolites are available, they have not received as much attention as the three previously described groups [52]. There are two main methods of deposition: spin coating and chemical vapor deposition (*CVD*) [52]. A few

promising low-k dielectric materials as well as the appropriate deposition techniques for each are listed in Table I.3 [16].

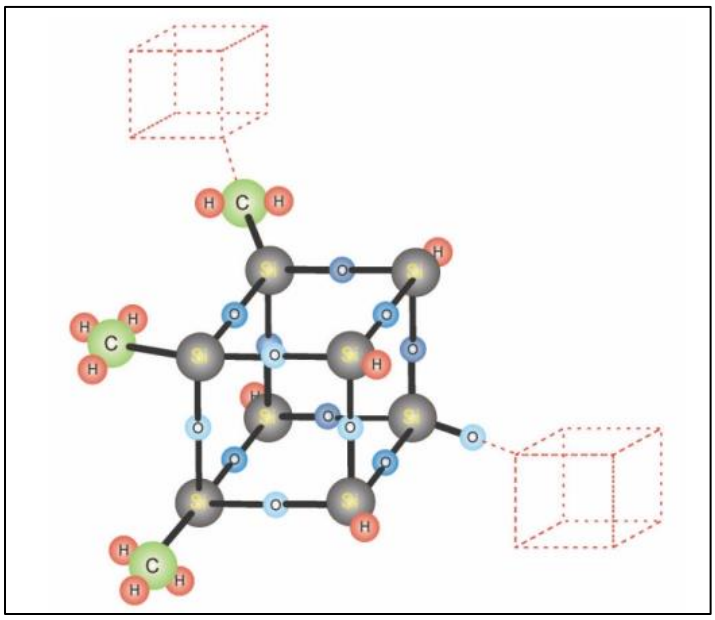

Figure I.10. *A schematic representation (not to scale) of a silsesquioxane (SSQ) unit [52].*

Table I.3. *Comparative analysis of deposition processes and dielectric constants of several low-κ dielectric materials [6].*

Dielectric material	Dielectric Constant	Deposition process
Silicon dioxide (SiO2)	3.8 − 3.9	PECVD
Carbon doped SiO2	2.2 − 2.7	PECVD
Bezocyclobutane (BCB)	2.49 − 2.65	Spin-on
HSSQ	2.9	Spin-on
MSSQ	2.7	Spin-on
Polyarelene (PAE)	2.8	Spin-on
Parylene-N	2.8	CVD
Parylene-F	2.3 − 2.5	CVD
Teflon AF	1.89 − 1.93	Spin-on
Diamond like carbon (DLC)	2.7 − 3.4	PECVD
Fluorinated DLC	2.4 − 2.8	PECVD
Aromatic thermosets (SiLK)	2.6 − 2.8	Spin-on

I.4.2 High - κ dielectric materials

The dielectric layer is one of the most esssential elements of a TFT that enables better miturisation of microelectronic devices. A thin dielectric layer is desired since a TFT's operating voltage is lower when the layer is thin. But if it gets too thin, the probability of developing pinholes rises. Additionally, the tunneling effect gets stronger, increasing the leakage current through the layer. High-κ dielectric materials can generate more charges with the same applied bias and layer thickness. The use of such materials can improve device performance by reducing gate leakage and improving gate capacitance [58].

Therefors, research activities have been directed towards discovering a material possessing a suitably high dielectric constant together with other important factors: band structure alignment with Si, film morphology optimisation, thermal stability [16,59]. Figure I.11 show the energy gap as a fuction of static dielectric constant for different dielectric materials. While the bandgaps and dielectric constants of various promising high-κ materials are listed in Table I.4.

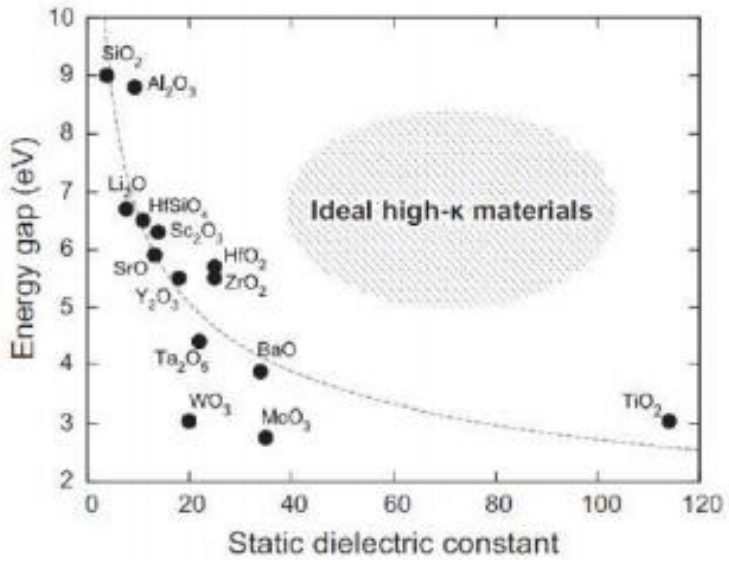

Figure I. 11. *Energy gap VS static dielectric constant for different Dielectric materials [58,65]*

Table I.4 *Band gaps and dielectric constants of various promising high-k materials*

Dielectric material	Band gap(eV)	Dielectric constant	Ref.
Si_3N_4	5	7.5	[60,61]
Al_2O_3	8.7	8.5-10.5	[60]
$ZrSiO_4$	~6	10-12	[60]
HfxSi1-xOy	6	15-25	[62]
ZrO_2	5.8	25	[60,63,64]
HfO_2	5.7	35	[63]
$LaAlO_3$	5.7	25	[65]
La_2O_3	4.3	27	[60,61]
Ta_2O_5	4-4.5	20-35	[60,64,66]
CeO_2	5.5	26	[31,60,67]
Y_2O_3	5.6	12-20	[68,69]
Nb_2O_5	4.06	50-200	[70,71,72]
TiO_2	3-3.5	30-100	[69,73,74]

1.5 CONCLUSION

This chapter has provided a literature survey of hydrogenated amorphous silicon and its well-established role in thin-film transistor technology. First, we summarized the fundamental properties of hydrogenated amorphous silicon: disordered structure, hydrogen incorporation, and electronic density of states. Then, we recalled the application of this semiconductor in field effect transistors behavior in electronic applications including the analysis of a-Si:H TFTs, operational principles, device physics, and performance characteristics, versatility and effectiveness in modern display technologies and electronic circuits. .Moreover, the chapter has addressed recent innovations, particularly the integration of Low-k and High-k dielectric materials, which open new avenues for performance enhancement and device scalability. Altogether, this chapter underscores the importance of a-Si:H as a central material in semiconductor research, applications for for future developments in thin-film electronics.

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CHAPTER II:

Silvaco Simulation Software & Its Validity

II.1 INTRODUCTION

This chapter consists of a comprehensive overview of the SILVACO system (tools, command structure, input/output handling, and the physical models) and its testing with experimetal data for a-Si:H. In fact, Silvaco Atlas makes use of a set of fundamental semiconductor equations: Poisson's equation, carrier continuity equations, and transport equations. In the case of amorphous materials such as a-Si:H, where disorder and defect states play a critical role, the simulator includes models that account for continuous distributions of localized states within the band gap. This approach enables a realistic representation of carrier transport, recombination, and generation processes in disordered systems. The second part of this chapter also concerns a comparative study between experimental data and simulation results for a-Si:H TFTs, focusing on key electrical characteristics such as transfer and output behavior. Importantly, this chapter has validated the accuracy and reliability of Silvaco Atlas in simulating the performance of a-Si:H TFTs. With this validation, the simulation can now be safely used to optimize device structures, predict electrical behavior, and support the design of high-performance thin-film transistors with results that closely reflect experimental observations.

II.2 SILVACO SIMULATION SOFTWARE

II.2.1 SILVACO System Description

Silvaco, founded in 1984 and headquartered in Santa Clara, California, is a leading company in TCAD (Technology Computer-Aided Design). It offers physics-based simulation tools that help design and predict the performance of semiconductor devices before fabrication. These tools are widely used in research and development to model devices accurately and efficiently. By incorporating advanced physical models, numerical algorithms, meshing techniques, and optimized solvers, Silvaco ensures that simulation results closely match practical outcomes [1]. It offers faster, cost-effective results compared to experiments, and it reveals insights that may be hard or impossible to measure directly [2].

II.2.2 SILVACO Tools

SILVACO is composed of several tools which were employed to simulate and analyze the performance of hydrogenated amorphous silicon thin-film transistors; they are:

- ✓ ***ATLAS:*** is a 2D/3D physically-based device simulator used to predict the electrical behavior of semiconductor devices and to explore internal physical mechanisms. It solves continuity and diffusion equations, supporting continuous, transient, and frequency-based analysis. It can be used independently or within the SILVACO framework [3].
- ✓ ***ATHENA:*** is a 2D process simulator for semiconductor fabrication. It enables structure definition and editing, including deposition, etching, and other technological steps involved in device processing [4].
- ✓ ***DeckBuild:*** is an interactive graphical environment for creating and managing input files for simulations. It simplifies mesh definition, mask application, and extraction processes, facilitating seamless transitions between simulators [5].
- ✓ ***DEVEDIT:*** is a device structure editor that allows mesh generation, structure modification, and device creation for simulation. It addresses issues with poor mesh quality by offering flexible mesh refinement tools and supports both GUI and DECKBUILD usage [6].
- ✓ ***TonyPlot:*** is a post-processing tool for visualizing simulation results. It integrates with SILVACO simulators and can be used independently or with tools like DeckBuild and VWF, providing detailed graphical analysis of output data [7].

II.3 APPLICATION OF SILVACO ATLAS TO a-SI:H TFTs

II.3.1 Basic Semiconductor Equations

Fondamentel understanding of physical phenomena of semiconductors materials as well semiconductor device beahavior are well expalined via well establshed mathematical

formula derived from Maxwell's laws. The most usual formula are : Poisson's equation, which relates charge density to electrostatic potential, and the continuity and transport equations, which describe carrier movement, generation, and recombination [9].

II.3.3.1 Poisson's Equation

Poisson's Equation relates the electrostatic potential to the space charge density [10]:

$$div(\varepsilon \nabla \psi) = -\rho \qquad \text{(II.1)}$$

where ψ is the electrostatic potential, ε is the local permittivity, and ρ is the local space charge density. The reference potential can be defined in various ways. For Atlas, this is always the intrinsic Fermi potential ψ_i which is defined in the next section. The local space charge density is the sum of contributions from all mobile and fixed charges, including electrons, holes, and ionized impurities.

The electric field is obtained from the gradient of the potential [10]:

$$\vec{E} = -\nabla \psi \qquad \text{(II.2)}$$

II.3.1.2 Carrier Continuity Equations

The continuity equations for electrons and holes are defined by equations [10]:

$$\frac{\partial n}{\partial t} = \frac{1}{q} div\overrightarrow{J_n} + G_n - R_n \qquad \text{(II.3)}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} div\overrightarrow{J_p} + G_p - R_p \qquad \text{(II. 4)}$$

where n and p are the electron and hole concentration, and are the electron and hole current densities, G_n and G_p are the generation rates for electrons and holes, R_n and R_p are the recombination rates for electrons and holes, and q is the magnitude of the charge on an electron. By default, Atlas includes both Equations (II.3) and (II.4).

II.3.1.3 Transport Equations

Calculations based on Boltzmann transport theory have shown that the current densities in the continuity equations can be defined by the drift-diffusion model [11]. In this model, the current densities are expressed as follows [10]:

$$\overrightarrow{J_n} = qn\mu_n\overrightarrow{E_n} + qD_n\nabla \mathrm{n} \qquad \text{(II.5)}$$

$$\overrightarrow{J_p} = qp\mu_p\overrightarrow{E_p} - qD_p\nabla \mathrm{p} \qquad \text{(II.6)}$$

Where D_n, D_p, $\mu_n$and μ_P are the diffusion coefficients and mobilities of electrons and holes, respectively, ∇n and ∇p gradient of electron concentration and holes, respectively, $\overrightarrow{E_n}$ and $\overrightarrow{E_p}$electric field acting on electrons and holes, respectively, and q is the elementary charge.

II.3.2 Basic Theory of Carrier Statistics

II.3.2.1 Fermi-Dirac and Boltazmann Statistics

Electrons in thermal equilibrium at temperature T_L with a semiconductor lattice obey Fermi Dirac statistics. That is the probability $f(\varepsilon)$ that an available electron state with energy ε is occupied by an electron is [10]:

$$f(\varepsilon) = \frac{1}{1+\exp(\frac{\varepsilon - E_F}{KT_L})} \qquad \text{(II.7)}$$

Where E_F is a spatially independent reference energy known as the Fermi level, T_L is the lattice temperature, ε is energy, and k is Boltzmann's constant.

II.3.2.2 Effective Density of states

The effective density of states in the conduction and the valence bands are expressed by the following theoretical expressions [10]:

$$N_C(T_L) = 2\left(\frac{2\pi m_e^* kT_L}{h^2}\right)^{\frac{3}{2}} = \left(\frac{T_L}{300}\right)^{\frac{3}{2}} NC300 \quad \text{(II.8)}$$

$$N_V(T_L) = 2\left(\frac{2\pi m_h^* kT_L}{h^2}\right)^{\frac{3}{2}} = \left(\frac{T_L}{300}\right)^{\frac{3}{2}} NV300 \quad \text{(II.9)}$$

Where m_e^* and m_h^* effective mass of electrons and holes, h Planck constant, k is Boltzmann's constant, T_L is the lattice temperature, and *NC300*,*NV300* are the effective density of states in the conduction band and valence band, respectively at a reference temperature of 300 K.

II.3.2.3 Intrinsic Carrier Concentration

The intrinsic carrier concentration (n_{ie}) is given for Boltzmann statistics by [10]:

$$n_{ie} = \sqrt{N_C N_V} exp\left(\frac{-E_g}{2kT_L}\right) \quad \text{(II.10)}$$

where N_C is effective density of states for electrons, N_V is effective density of states for holes, E_g is the band-gap energy, T_L is the lattice temperature, and k is Boltzmann's constant.

II.3.2.3 Density of states in amorphous semiconductors

Amorphous semicondcutors are charaterised by a continuous spectrum of defects and consequently a density of localised states in the enrgy gap. Silvaco Atlas supports the simulation of disordered material systems and complex Thin-Film Transistor structures by enabling the definition of continuous defect states within the band gap of amorphous semiconductors [2]. Thus, it is posssible to accurately simulate materials like a-Si:H, a-InGaZnO (IGZO) and a-InSnZnO (ITZO), which contain a large density of defect states. Hence, accurate simulations require a continuous density of states model with band tails near the condcution band edge or near the valence band edge as well as deep density of states in the middle of the bandgap [8].

II.3.3 Atlas inputs and outputs

Figure II.1 depicts the categories of information that flow in and out of Atlas [3]. Atlas simulations employ two input files:

- ✓ ***A text file:*** That contains commands for Atlas to execute.
- ✓ ***Structure file****:* That defines the structure that will be simulated.

Atlas generates three distinct types of output files [3]:

- ✓ ***Run-time output****:* This provides real-time updates on the simulation's progress, along with error and warning messages as the simulation advances.
- ✓ ***Log file****:* The log file archives all terminal voltages and currents stemming from the device analysis
- ✓ ***Solution file****:* This file stores two-dimensional (2D) and three-dimensional (3D) data, encompassing the values of solution variables within the device at a specific bias point .

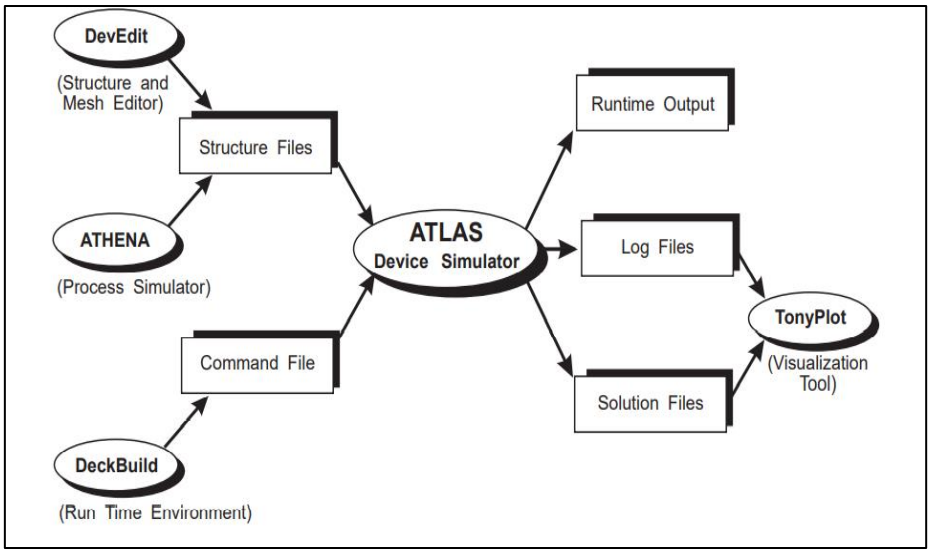

Figure II.1. *Atlas inputs and outputs [3].*

II.3.4 Order of Atlas commands

The order of statements within an Atlas input file is of utmost importance. It includes five distinct groups, as regrouped in Table II.1, which require precise sequencing. Deviating from this order can trigger an error message, potentially causing erroneous operation or program termination. For instance, incorrect arrangement of material parameters or models might lead to their exclusion from the calculations. Moreover, the statement order within the mesh definition, structural definition, and solution groups is critical to avert incorrect operation or program termination [3].

Table II.1. *Atlas command groups with the primary statements in each group [3].*

Group	Statements
Structure specification	Mesh, Region, Electrode, Doping
Material models specification	Material, Models, Contact, Interface
Numerical method Selection	Method
Solution specification	Log, Solve, Load, Save
Results analysis	Extract, Tonyplot

II.4 Validity and Accuracy of Simulation

II.4.1 a-Si:H TFT structure and parameters

Figure II.2 illlsutrates a across-sectional view of a hydrogenated amorphous silicon thin-film transistor. The structure is based on a real technologically realized design and consists of several layers deposited on a glass substrate [12]. This device is composed of different elements and materials which are cited below:

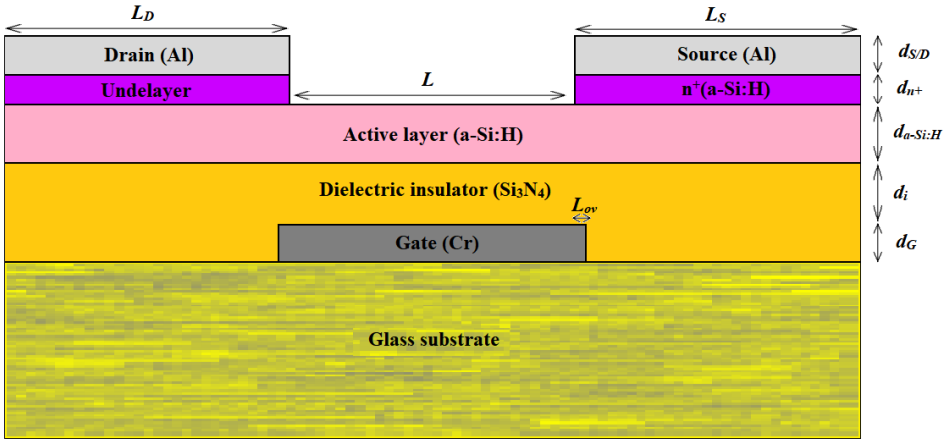

Figure II.2. *Cross section of an a-Si:H TFT structure, with its main geometrical parameters, used for numerical simulation*

- ✓ ***Substrate:*** The device is built on a glass substrate.
- ✓ ***Gate Electrode (G):*** A chromium (Cr) film is deposited on the glass substrate and etched to form the gate electrode.
- ✓ ***Gate Insulator:*** A 0.3 µm thin layer of silicon nitride (Si_3N_4) is used as the gate insulator.
- ✓ ***Active Layer:*** The amorphous silicon (a-Si) serves as the semiconducting active layer.
- ✓ ***Underlay (n+ a-Si:H):*** A very thin layer of heavily doped hydrogenated amorphous silicon (n^+ a-Si:H) is added to reduce contact resistance between the metal and the a-Si:H layer and to improve electron injection properties [12]. The doping concentration of this layer is set to 8.10^{18} /cm^3.
- ✓ ***Top Metallization:*** Aluminum (Al) is deposited as the top metallization to form the source (S) and drain (D) electrodes in a planar configuration.
- ✓ ***Overlap Length (L_{ov}):*** There is an overlap length of 1 µm between the gate electrode and the drain-source electrodes.
- ✓ The dielectric layer (Si_3N_4) and the glass substrate have specific properties, including energy gaps and permittivities:
- ✓ ***Dielectric layer (Si3N4):*** Energy gap of 5.3 eV and a permittivity of 7.5 [13].
- ✓ ***Glass Substrate:*** Energy gap of 9 eV and a permittivity of 3.9 [14].

The main geometrical parameters of the a-Si:H TFT device are summarized in Table II.2. Additional characteristics and parameters of the semiconducting active layer (a-Si:H) can be found in Table II.3.

Table II.2. *Values of geometric and technological parameters for a-Si: H TFT.*

Parameter	Material	Thickness (nm)		Length (µm)		Width (µm)	
		Symbol	Value	Symbol	Value	Symbol	Value
Gate electrode	Cr	d_G	200	L_G	4	W_G	500
Gate insulator	Si_3N_4	d_i	300	L_i	2	W_i	500
Source-drain electrodes	Al	$d_{S/D}$	200	$L_{S/D}$	4	$W_{S/D}$	500
Source-drain underlay	n^+(a-Si:H)	d_{n+}	25	L_{n+}	4	W_{n+}	500
Active layer	a-Si:H	$d_{a\text{-}Si:H}$	300	$L_{a\text{-}Si:H}$	2	$W_{a\text{-}Si:H}$	500

Table II.3. *Electrical parameters of a-Si:H.*

Parameter	Symbol	Unit	a-Si:H	Ref.
Band gap	E_g	eV	1.8	[15]
Permittivity	ε		11.9	[15, 16]
Conduction band Density	N_c	cm^{-3}	$2.5x10^{20}$	[15]
Valence band Density	N_v	cm^{-3}	$2.5x10^{20}$	[15]
Electron mobility	μ_n	cm^2/Vs	20	[15]
Hole mobility	μ_h	cm^2/Vs	0.12	[17]
Electron life time	τ_n	s^{-1}	$1 x10^{-6}$	[18]
Hole life time	τ_h	s^{-1}	$1 x10^{-6}$	[18]
Electronic affinity	X	eV	4	[16, 19]

II.4.2 Experiment versus Simulation of a-Si:H TFT performance

II.4.2.1 DC current-voltage characteristics

In the study of thin-film transistors, two principal electrical characteristics are commonly analyzed: the transfer characteristics and the output characteristic. These characteristics provide valuable insights into the behavior and performance of the TFT under different biasing conditions.The simulated transfer and output characteristics are compared to experimental measurements taken from real fabricated a-SI:H TFTs [12].

a)Transfer characteristics

Figure II.3 shows the transfer characteristics (drain current-gate voltage, I_{DS}-V_{GS}) of a hydrogenated amorphous silicon thin-film transistor obtained numerically through simulation (continuous lines). The transfer characteristics are plotted semi-logarithmically, showing the source-drain current (I_{DS}) as a function of the gate voltage (V_{GS}) for different drain potentials (V_{DS}) of 2 V, 10 V, and 20 V.

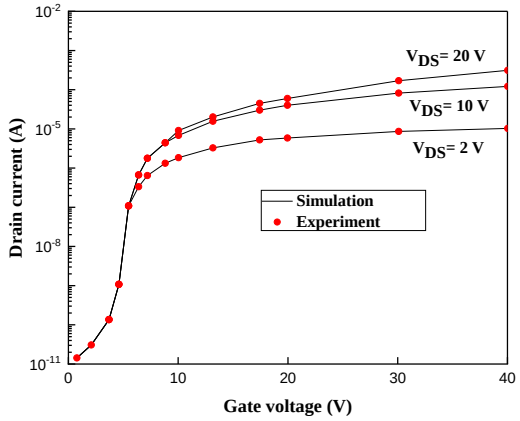

Figure II.3. *Calculated (—) and Experimental (● ● ●)[12] transfer characteristics of a-Si: H TFT for different drain potentials: V_{DS} = 2V, 10V and 20V.*

The curves exhibit the typical behavior of an TFT transfer characteristic. As the gate voltage (V_{GS}) increases, the drain current (I_{DS}) shows an initial slow variation, followed by a sharp increase, and finally, a quasi-saturation region. This behavior is a characteristic of

TFTs and is due to the formation of an electron accumulation layer at the Si/Si_3N_4 interface, which effectively shorts out the high resistance between the source and drain electrodes [12].

The simulation results are compared to experimental data (marked with ● ● ●) obtained from [12]. The text mentions that the agreement between the simulation and experimental data is extremely good, indicating that the simulation model accurately captures the real behavior of the a-Si:H TFT.

The comparison of the simulated and experimental curves reveals interesting results. As the voltages increase, the drain currents also increase. At the "off " condition (V_{GS} = 0), the drain current is very low (I_{DS} = 10^{-11} A), indicating minimal or no current flow between the source and drain electrodes. As the gate voltage is raised (V_{GS} ≈ 5 V), the drain current reaches 1 µA, and for higher voltages, it goes up to a fraction of mA. This behavior suggests that the a-Si:H TFT can achieve high I_{on}/I_{off} ratios, which are ratios of the drain-source current (I_{on}) to the off-current (I_{off}). The I_{on}/I_{off} ratios obtained are higher than the values typically obtained (> 10^6) for thin film transistors, reaching values higher than 10^8. The high I_{on}/I_{off} ratios obtained in a-Si:H TFTs are encouraging for their potential applications in electronic switching devices, where the ability to achieve a significant difference between the off-state and on-state currents is crucial for efficient and reliable device operation.

b)Output characteristics

Figure II.4 represents the output characteristics (drain current-drain voltage, I_{DS}-V_{DS}) of the hydrogenated amorphous silicon field-effect transistor with the same structure as previously investigated. The output characteristics are plotted linearly, showing the source-drain current (I_{DS}) as a function of the source-drain voltage (V_{DS}) for different typical gate voltages (V_{GS}) of 2 V, 16 V, and 20 V.

The curves in Figure II.4 exhibit two distinct regions of variation:

(i) Initial Linear Regime: At lower values of source-drain voltage (V_{DS}), the drain current (I_{DS}) shows a linear response with respect to V_{DS}. This linear region corresponds to the device

operating in its "linear" or "ohmic" region, where the current is directly proportional to the applied voltage.

(ii) Saturated Regime: For higher values of source-drain voltage (V_{DS}), the drain current (I_{DS}) reaches a saturation point and no longer increases significantly with further increases in V_{DS}. This saturation is a characteristic of the device operating in its "saturation" region.

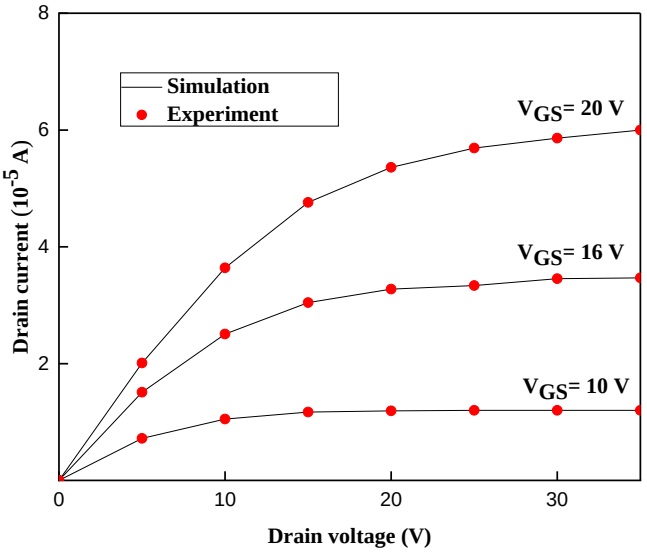

Figure II.4. *Calculated (—) and Experimental (● ● ●) [12] Output characteristics of a-Si:H TFT for V_{GS} = 10, 16 and 20 Volts.*

The saturation regions in the output characteristics indicate that the a-Si:H TFT is effectively limiting the current flow due to the channel reaching its maximum current-carrying capacity. As the gate voltage (V_{GS}) is increased, the drain current in the saturation region also increases. The drain currents achieved in the saturation region are reported as 1.2×10^{-5} A, 3.5×10^{-5} A, and 6.2×10^{-5} A for gate voltages of 10 V, 16 V, and 20 V, respectively.

The simulation results of the output characteristics are compared to experimental data (marked with ● ● ●) obtained from [12]. The agreement between the simulation and experimental data is good, suggesting that the simulation accurately captures the real behavior of the a-Si:H TFT in terms of output characteristics.

Therefore, the output characteristics investigation confirms that the a-Si:H TFT exhibits expected behavior, with distinct linear and saturation regions as V_{DS} and V_{GS} are varied. The agreement with experimental data validates the simulation model and indicates that the a-Si:H TFT can achieve good performances for potential applications in electronic devices.

II.4.2.1 Transistor main electrical parameters

Based on the DC current-voltage characteristics obtained from the simulation of the investigated hydrogenated amorphous silicon thin film ransistor structure (Figure III.1), the following performance parameters have been determined at V_{DS} = 2 V: threshold voltage = 4.86 V, field-effect mobility = 0.098 $cm^2V^{-1}s^{-1}$, subthreshold swing = 0.47 V/decade, on-state current = $1.02x10^{-5}$ A, off-state current = $1.29x10^{-11}$ A, I_{on}/I_{off} = $0.79x10^6$, capacitance per unit area, C_i = $2.21x10^{-8}$ Fcm^{-2}, and electrical resistivity, ρ_e = $1.60x10^4\Omega$.cm of the active layer of the a-Si:H TFT device.

These performance parameters provide valuable insights into the a-Si:H TFT's behavior and suitability for various electronic applications. The good agreement between the simulation and experimental results further validates the accuracy and applicability of this software in predicting the device's performance, and support the next simulation results.

II.5 CONCLUSION

The SILVACO simulation software was recalled in this chpter, with a particular focus on Silvaco Atlas and its application to the simulation of a-Si:H TFTs. The essential mechanisms of the SILVACO system, including the key tools and input-output parameters necessary for effective simulation. The relevent semiconductor equationswere discussed. Moreover, the validity, the accuracy and reliability of Silvaco Atlas in simulating the performance of a-Si:H TFTs were put into evidence through detailed comparisons of experimental and simulated data, particularly in terms of DC current-voltage characteristics and key transistor parameters. With this validation, the simulation can now be safely used to optimize device structures, predict electrical behavior, and support the design of high-performance thin-film transistors with results that closely reflect experimental observations.

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CHAPTER III:

Results & Discussions

III.1 INTRODUCTION

In this chapter, we present the results and discussions obtained from a detailed investigation of a-Si:H TFT structures and parameters. In order to optimise the perfomances of such devices.These results are analyzed, quantified and validated through simulation and comparative studies. To do so, we considered the most important parameters: (i) the gate dielectric thickness, (ii) the dielectric constant (κ), and (iii) the active layer thickness. To do so, we first chose the scaling down film thicknesses from 300 to 15 nm for both dielctric and active layers then we considered a great number of dielectric materials: Strontium Titanate ($SrTiO_3$), Barium Strontium Titanate ($BaSrTiO_3$), Strontium Zirconate ($SrZrO_3$), Niobium Pentoxide (Nb_2O_5), Titanium Dioxide (TiO_2), Hafnium Dioxide (HfO_2), Tantalum Pentoxide (Ta_2O_5), Lanthanum Oxide (La_2O_5), Cerium Dioxide (CeO_2),Zirconium Dioxide (ZrO_2),Gadolinium Oxide (Gd_2O_5),Yttrium Oxide (Y_2O_3), Aluminum Oxide (Al_2O_3), Silicon Nitride (Si_3N_4), Silicon Dioxide (SiO_2). In all cases, we deduced the effects of such parameters on elctrical transfer and output characteristics. From these charateristics, we determined and quantified the variations of threshold voltage, capacitance per unit area, field-effect mobility, subthreshold swing, and *Ion/Ioff* ratio with film thiknesses and dielecric constants. Finally, to contribute to the advancement of thin-film transistor technology and its potential applications in various electronics barnches, we propose the most optimised design with the best performances of a-Si:H TFTs

III.2 EFFECTS OF THE GATE DIELECTRIC THICKNESS

III.2.1 Qualitative observations

Figure III.1 illustrates the semi-logarithmic plots of the transfer characteristics of the investigated hydrogenated amorphous silicon Tin-Film-Transistor at V_{DS} = 2 V, for different gate dielectric (Si_3N_4) thicknesses. The plots include a large spectrum of thicknesses ranging from 300 nm down to 15 nm.

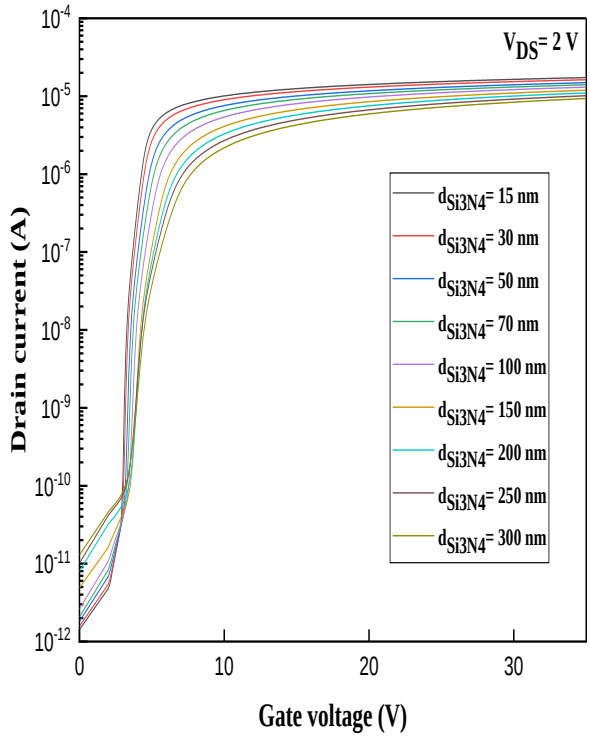

Figure III.1. *Transfer characteristics of a-Si: H TFT for different Si_3N_4 gate dielectric thicknesse*

The behavior of all the curves is consistent with standard transistor characteristics and exhibits the following observations:

- ✓ ***Initial slow increase:*** As the gate voltage (V_{GS}) increases from the off-state, the drain current (I_{DS}) shows a gradual and slow rise at the beginning.
- ✓ ***Very sharp increase:*** Following the initial slow increase, there is a sharp and rapid increase in the drain current as the gate voltage continues to rise. This behavior is typically observed as the transistor enters the "on" state, and the channel starts conducting a significant amount of current.
- ✓ ***Final quasi-saturation region:*** After the sharp increase, the drain current reaches a saturation point, and the rate of increase becomes much slower. The transistor operates in its "saturation" region, and further increases in the gate voltage have little effect on the drain current.

However, as the thickness of the gate dielectric (Si_3N_4) changes, the plots show some notable discrepancies:

- ✓ ***Onset of off-state variation***: Thinner Si_3N_4 layers show an earlier onset of the initial variation corresponding to the off-state. This means that the drain current starts to increase at lower gate voltages for thinner gate dielectric thicknesses, indicating improved switching behavior.
- ✓ ***Sharpness of the increase:*** Thinner gate dielectric thicknesses exhibit a sharper increase in drain current with increasing gate voltage. This sharper increase suggests better gate control and enhanced performance in the "on" state.
- ✓ ***Saturated drain current:*** The saturated drain current values, which correspond to the on-state current, are higher for thinner gate dielectric thicknesses. This indicates that thinner dielectric layers allow for higher current-carrying capacity and improved overall performance.
- ✓ ***Transition region:*** The transition region between the off-state and on-state becomes narrower for thinner Si_3N_4 layers. This narrower transition region suggests that the a-Si:H TFT achieves a sharper and more well-defined switching behavior.

These qualitative observations indicate that the a-Si:H TFT characteristics improve as the gate dielectric becomes thinner. Thinner gate dielectric layers result in better switching behavior, higher drain current in the on-state, and enhanced overall performance of the transistor. These findings are significant as they highlight the importance of gate dielectric thickness in optimizing the performance of a-Si:H TFTs, and they offer valuable insights for device design and fabrication to achieve desired characteristics for specific electronic applications.

Figure III.2 shows a set of typical output characteristics of the hydrogenated amorphous silicon field-effect transistor plotted linearly in terms of drain current (I_{DS}) versus drain-source voltage (V_{DS}) at a constant gate voltage (V_{GS}) of 10 V. The plots show results for various gate dielectric thicknesses, ranging from 300 nm down to 15 nm (300, 250, 200, 150, 100, 70, 50, 30 and 15 nm)

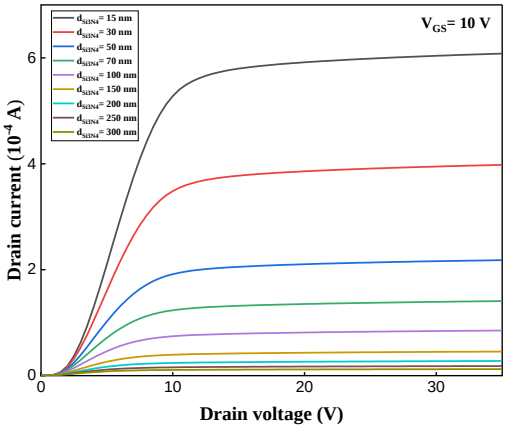

Figure III.2. *Output characteristics of a-Si;H TFT, at V_{GS} = 10 V, for different Si_3N_4 gate dielectric thicknesses.*

The behavior of all the curves in Figure III.2 shows a similar pattern, characterized by two regions:

- ✓ ***Initial increase:*** At lower values of drain-source voltage (V_{DS}), the drain current (I_{DS}) shows an initial increase as V_{DS} is raised. This initial increase in drain current is observed when the transistor is in its "linear" or "ohmic" region of operation.
- ✓ ***Saturation region:*** After the initial increase, the drain current reaches a saturation point and does not increase significantly with further increases in V_{DS}. The transistor enters its "saturation" region, and the drain current becomes relatively constant at higher V_{DS} values.
- ✓ As the gate dielectric thickness decreases, several notable changes are observed in the output characteristics:
- ✓ ***Increase in slope:*** The slope in the initial increase region becomes steeper for thinner gate dielectric thicknesses. This means that for smaller dielectric thicknesses, the transistor exhibits a more rapid increase in drain current as V_{DS} is raised.
- ✓ ***Higher drain current in saturation:*** The drain current in the saturation region increases as the gate dielectric becomes thinner. Thinner gate dielectric layers allow for higher current-carrying capacity, resulting in higher drain currents in the saturated region.

These observations suggest that as the gate dielectric thickness decreases, the a-Si:H TFT exhibits improved performance in terms of output characteristics. The steeper slope in the initial region indicates better conduction and enhanced response to variations in V_{DS}. The higher drain current in the saturation region indicates a higher current-carrying capacity and better saturation behavior.

These phenomena asssociated with the influence of gate dielectric thickness on the output characteristics of the a-Si:H TFT provide valuable insights for optimizing device performance and understanding the role of gate dielectric thickness in a-Si:H TFT design. They also offer useful information for tailoring the device characteristics to meet specific application requirements, such as in electronic switching devices or other applications.

III.2.1 Quantification of Si_3N_4 thickness effects

Table III.1 contains the obtained numerical results for various performance parameters of the hydrogenated amorphous silicon field-effect transistor for different gate dielectric thicknesses. All the parameters considered in the table vary with the gate dielectric thicknesses.

Table III.1. *Deduced parameter values for a-Si:H TFT for different Si_3N_4 gate thicknesses*

d_i (nm)	C_i (10^{-8} F/cm^2)	V_T (V)	μ_{FE} (cm^2/Vs)	I_{on} (10^{-5} A)	I_{off} (10^{-11} A)	I_{on}/I_{off} ($\times 10^6$)	SS (V/dec.)
300	2.21	4.86	0.098	1.02	1.29	0.79	0.47
250	2.65	4.57	0.096	1.10	1.01	1.08	0.40
200	3.31	4.43	0.094	1.18	0.80	1.48	0.33
150	4.42	4.24	0.089	1.27	0.49	2.59	0.27
100	6.63	3.85	0.081	1.38	0.26	6.66	0.21
70	9.48	3.58	0.075	1.48	0.21	7.05	0.17
50	13.27	3.38	0.068	1.57	0.18	8.72	0.15
30	22.12	3.17	0.058	1.70	0.15	11.33	0.11
15	44.25	3.06	0.037	1.81	0.14	12.81	0.10

The variations in the parameters with dielectric thicknesses are in line with the above qualitative observations As the gate dielectric thickness decreases, certain key performance parameters show improvements, indicating enhanced device behavior:

- ✓ The capacitance per unit area increases for thinner gate dielectrics, indicating higher gate control efficiency.
- ✓ The threshold voltage change with dielectric thickness, affecting the on/off behavior of the transistor.
- ✓ The field-effect mobility can be affected by the dielectric thickness, indicating how effectively carriers move in the channel.
- ✓ The on-state current shows variations, suggesting changes in the current-carrying capability of the device.
- ✓ The off-state current changes with dielectric thickness, indicating the leakage current in the off-state.
- ✓ The I_{on}/I_{off} ratio, representing the switching performance, might vary significantly.
- ✓ The subthreshold swing that characterizes the steepness of the transistor's switching behavior and also shows variations.

Therefore, the changes in the performance parameters of the a-Si:H TFT with different gate dielectric thicknesses clearly establish their– sensitivity to variations in the gate dielectric. This behaviour highlights the importance of precise controls the dielectric layer during device fabrication. Thus, this result can be used to optimize the device performance, design considerations, and understand the trade-offs involved in choosing appropriate gate dielectric thicknesses for specific applications. It also serves as a valuable reference for future studies and advancements in a-Si:H TFT technology.

Figure III.3 illustrates the effects of different gate dielectric thicknesses (ranging from 15 nm to 300 nm) on various key parameters of the hydrogenated amorphous silicon field-effect transistor. The parameters analyzed in the plots include (i), Threshold Voltage (Figure III.3.a) , (ii) Capacitance per Unit Area (Figure III.3.b), (iii) Field Effect Mobility (Figure III.3.c), (iv) Subthreshold Swing (Figure III.3.d) and (v) I_{on}/I_{off} Ratio (Figure III.3.e).

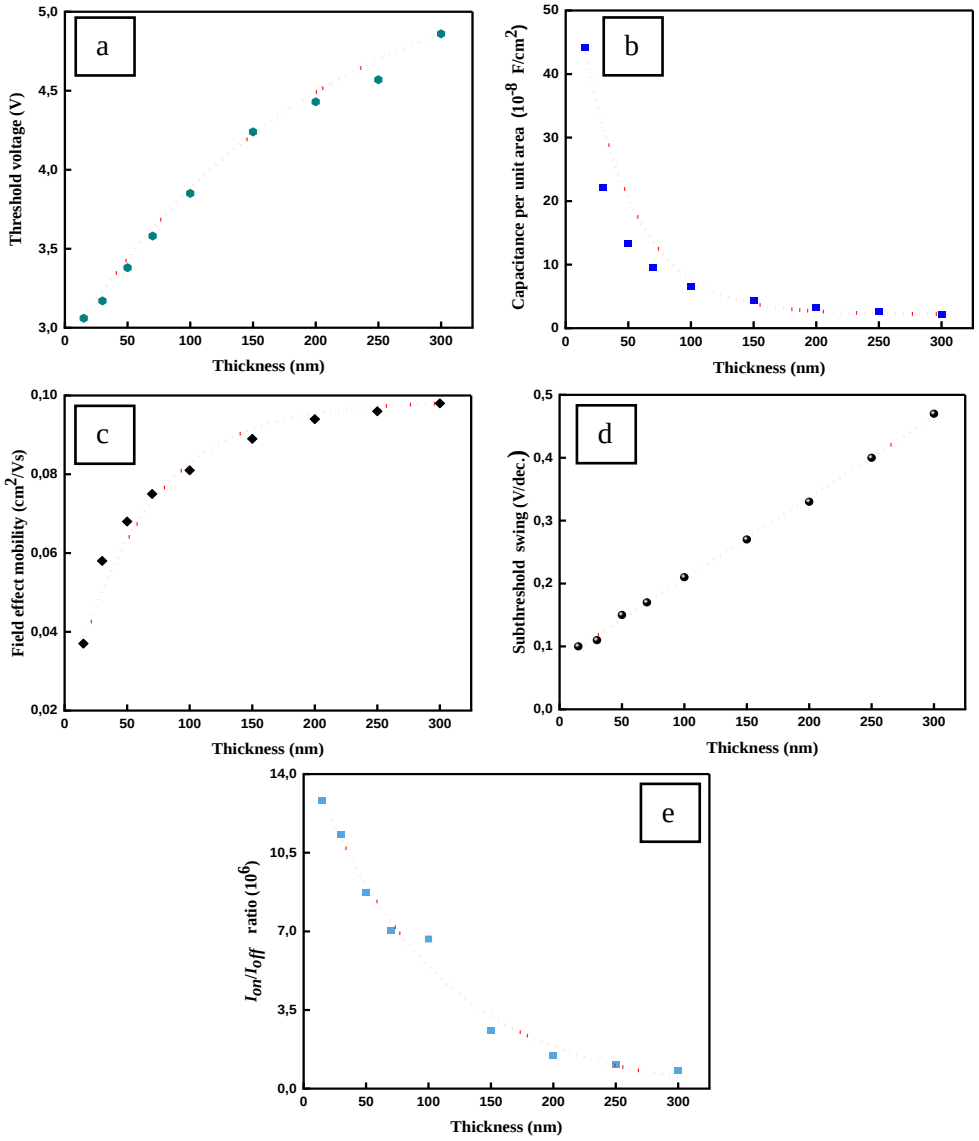

Figure III.3. *Effects of Si_3N_4 thicknesses on: (a) Threshold voltages, (b) Capacitance per unit area, (c) Field effect mobility, (d) Subthreshold swing and (e) I_{on}/I_{off} ratio.*

As the gate dielectric thickness (d_i) increases, the behaviors of these parameters are quantified through curve fitting, represented by the dotted lines (....) in Figure III.3. The lines of best fit provide insights into how each parameter varies with the change in dielectric thickness. The deduced realtions of every parameter as a fuction of dielectric thickness in the range 15 to 300 nm are detailed belw.

✓ Threshold voltage (Figure III.3.a) increases from 3.06 to 4.86 V as a results of the large increase of the current caused by the increase of the capacitive injection of free charge carriers (electrons); it follows an exponential variation (….) with thickness of the form:

$$V_T = 5.42 - 2.55 \exp(-0.005\, d_i) \quad \text{(III.1)}$$

✓ Capacitance per unit area (Figure III.3.b) decreases from 22.12×10^{-8} to 2.21×10^{-8} Fcm^{-2} with increasing the dielectric thickness; it follows an exponential variation (….) of the form:

$$C_i = 2.16 + 60.23 \exp(-0.023\, d_i) \quad \text{(III.2)}$$

✓ Field-effect mobility (Figure III.3.c) slightly increases from 0.037 to 0.098 $cm^2V^{-1}s^{-1}$, this can be attributed to the heightened capacitance per unit area and the reduction in the maximum slope of the transfer characteristic in the linear plot. The parameter μ_{FE} follows an exponential variation (….) with thickness of the form:

$$\mu_{FE} = 0.098 - 0.078 \exp(-0.015\, d_i) \quad \text{(III.3)}$$

✓ The subthreshold swing (Figure III.3.d) increases from 0.10 to 0.47, due to the augmentation in the maximum slope of the transfer characteristic, which stems from an increase in the drain current. The quantification of this parameter (….) gave following relation:

$$SS = 0.079 + 0.001\, d_i \quad \text{(III.4)}$$

It should be noted that a small subthreshold swing (corresponding to a lower voltage/decade obtained for the 15 nm thick gate insulator) is more desirable for achieving fast switching time between the on- and off-states. The subthreshold swing reflects the dielectric/semiconductor interface quality of a metal oxide TFT.

✓ I_{on}/I_{off} ratio (Figure III.3.e) decreases from 12.81×10^6 to 0.79×10^6 due to the increase in drain current, and the decrease in the off-state which results from an increased capacitance per unit area. This ratio follows an exponential variation (….) with thickness of the form:

I_{on}/I_{off}=-0.31+15.27 exp(-0.010 d_i) (III.5)

Moreover, it is worth noting that the on-state current, $I_{on,}$ decreases from 1.81x10^{-5} to 1.02x10^{-5} A. Whereas, I_{off}, increases from 0.14x10^{-11} to 1.29x10^{-11} A. Both parameters vary exponentially as follows:

I_{on}=0.93+0.99 exp(-0.008 d_i) (III.6)

I_{off}=-0.50+0.57 exp(-0.004 d_i) (III.7)

These deduced expressions provide quantitative insights into how these key parameters of the a-Si:H TFT change with varying gate dielectric thicknesses. The curve fitting analysis allows for a better understanding of the dependence of these parameters on the dielectric thickness, which is crucial for optimizing the device performance and designing a-Si:H TFTs for specific applications.

From the analysis of a-Si:H TFTs with different gate dielectric (Si_3N_4) thicknesses (Figure III.3), it can be concluded that TFTs with lower thicknesses exhibit better electrical characteristics in terms of threshold voltages, capacitance per unit area, field effect mobility, subthreshold swing, off-state currents, on-state currents, and *Ion/Ioff* ratio. Thinner gate dielectric layers result in improved transistor performance, as indicated by the various parameters studied.

Moreover, a close analysis of the deduced relations (Eq.III.1 to III.7) reveals that, except for the subthreshold swing which shows a linear variation with dielectric thickness (Eq.III.4), all other investigated TFT electrical parameters (C_i, V_T, μ_{FE}, I_{on}, I_{off}, I_{on}/I_{off}) follow a similar exponential dependence of the form:

$P=P_0+\alpha\exp(\beta d_i)$ (III.8)

Where P_0, α, and β are specific constants that describe the variation of the given parameter with dielectric thickness. The values of these constants are summarized in Table

III.2. The units indicated in the table refer to their corresponding a-Si:H TFT parameters, while α and β are unitless constants.

Table III.2. *Characteristic constant values in the relationship $P = P_0 + \alpha exp(\beta d)$ for all a-Si:H TFT electrical parameters where P represents (C_i, V_T, μ_{FE}, I_{on}, I_{off}, and I_{on}/I_{off}).*

P	C_i (10^{-8} F/cm^2)	V_T (V)	μ_{FE} (cm^2/Vs)	I_{on} (10^{-5} A)	I_{off} (10^{-11} A)	I_{on}/I_{off} $\times 10^6$
P_0	2.16	5.42	0.10	0.93	- 0.50	- 0. 31
α	60.23	- 2.55	- 0.06	0.99	0.57	15.27
β	-0.023	0.006	- 0.015	- 0.008	-0.004	- 0.010

This exponential relations (Eq.III.8) gives a straightforward determination of a desired parameter (C_i, V_T, μ_{FE}, I_{on}, I_{off}, I_{on}/I_{off}) for a given a-Si:H TFT with known dielectric thickness. If the dielectric thickness is known, one can use the constants α and β from the table to determine the specific parameter of interest. Similarly, if any of these parameters (C_i, V_T, μ_{FE}, I_{on}, I_{off}, I_{on}/I_{off}) is measured experimentally for an a-Si:H TFT, one can use Eq.III.8 to deduce the exact Si_3N_4 thickness of the investigated device. This provides a useful tool for device characterization and optimization, as well as for identifying the dielectric thickness in fabricated a-Si:H TFTs. Therefore, the analysis of the exponential dependence of a-Si:H TFT electrical parameters on gate dielectric thickness offers valuable insights into device behavior and optimization. The determined relations permits the determination of specific parameters based on dielectric thickness and vice versa.

III.3 EFFECTS OF THE GATE DIELECTRIC MATERIALS

Gate dielectric materials, charcterised by dielectric constants (κ), play a crucial role in the performance any field effect transistor To quantify the influence of this parameter on the performances of hydrogenated amorphous silicon FETs, several dielectric materials (Table III.3) were chosen ($SrTiO_3$, $BaSrTiO_3$, $SrZrO_3$, Nb_2O_5, TiO_2, HfO_2, Ta_2O_5, La_2O_5, CeO_2, ZrO_2, Gd_2O_5, Y_2O_3, Al_2O_3, Si_3N_4, and SiO_2), with different dielectric constants (κ) values ranging from 3.9 (for SiO_2) to 300 (for $SrTiO_3$)..

Table III.3. *Different gate dielectric materials with their dielectric constants and gap energies.*

Dielectric material	Dielectric Constant	Ebeegy Gap (eV)
SiO_2	3.9 [8,20]	9 [8,20]
Si_3N_4	7.5 [8,21]	5 [8]
Al_2O_3	9.5 [20]	8.7 [4,8,20]
Y_2O_3	16 [8,20]	5.6 [8,20]
Gd_2O_5	18 [8]	5.4 [8]
ZrO_2	25 [9,20]	5.8 [8,9,20,22]
CeO_2	26 [8]	5.5 [8]
La_2O_3	27 [8]	4.3 [8]
Ta_2O_5	27.5 [8,20]	4.25 [8,20]
HfO_2	35 [8]	5.7 [8,20]
TiO_2	65 [8]	3.25 [8,20]
Nb_2O_5	125 [8]	4.06 [8]
$SrZrO_3$	180 [8]	5.4 [8]
$BaSrTiO_3$(BST)	250 [8]	3.21 [8,23]
$SrTiO_3$	300 [8]	3.27 [8,24]

III.3.2 Device Characteristics

III.3.2.1 Qualitative observations

Figure III.4 illustrates the semi-logarithmic plots of the deduced transfer characteristics of the hydrogenated amorphous silicon field-effect transistor (a-Si:H TFT) at V_{DS} = 2 V, for different gate dielectric materials. The gate dielectric materials considered in the plot include: $SrTiO_3$, $BaSrTiO_3$,$SrZrO_3$, Nb_2O_5, TiO_2, HfO_2, Ta_2O_5, La_2O_5, CeO_2, ZrO_2, Gd_2O_5, Y_2O_3, Al_2O_3, Si_3N_4, and SiO_2. The choice of dielectric materials depends on several factors such as device performance requirements, process compatibility, and fabrication restrictions

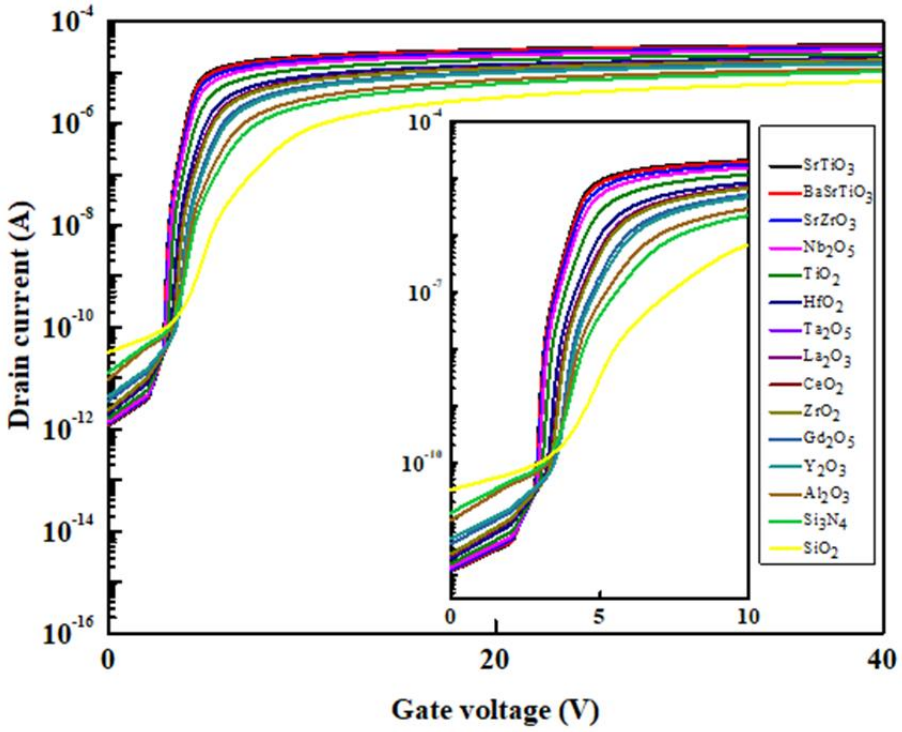

Figure III.4. *Transfer characteristics of a-Si: H TFT for different gate dielectric materials.*

The transfer characteristics are plotted semi-logarithmically, showing the source-drain current (I_{DS}) as a function of the gate voltage (V_{GS}) for each of the different gate dielectric materials. The purpose of this analysis is to compare the effects of using various gate dielectric materials on the behavior and performance of the a-Si:H TFT. Different gate dielectrics can significantly influence the transistor's electrical characteristics, such as threshold voltage, field effect mobility, on- and off-state currents, and switching behavior.

By comparing the transfer characteristics of the a-Si:H TFT with different gate dielectric materials, researchers can gain insights into the suitability of each material for particular device requirements and explore potential enhancements in device performance. This comparative analysis aids in the optimization of a-Si:H TFT design and provides valuable information for advancing the technology and application of thin-film transistors in various electronic devices and systems. The transfer characteristics of a-Si:H TFT, at V_{DS} = 2 V, for different gate dielectric materials indicate that as the dielectric constant (k) increases from 3.9 to 300, several effects can be observed:

- ✓ ***Increased Drain Current***: With the increase in dielectric constant, the drain current of the a-Si:H TFT tends to rise from I_{DS} = 6.63x10^{-6}A, to 3.5x10^{-5} A. This suggests that a higher dielectric constant enhances the flow of current through the device.
- ✓ ***Enhanced Performance***: The enhancement in the dielectric constant results in notable improvements in the electrical characteristics and overall performance of the a-Si:H TFT. This advancement can be attributed to the reduction in the electrical thickness of the gate dielectric, leading to an improved gate capacitance per unit area.

It is important to note that these observations are specific to the mentioned conditions (V_{DS} = 2 V) and the investigated gate dielectric materials. Other factors such as material properties, device dimensions, and operating conditions can also influence the transfer characteristics and performance of a-Si:H TFTs with different gate dielectric materials.

Figure III.5 illustrates a typical set of deduced curves of the a-Si:H TFT output characteristics plotted linearly in terms of I_{DS} versus V_{DS} at V_{GS} = 10 V for different gate dielectric materials.

It can clearly be seen that all the curves show an initial linear increase followed by a saturation region. The output characteristics of a-Si:H TFT, at V_{GS} = 10 V, for different gate dielectric materials show that the increase in the dielectric constant (K) from 3.9 to 300, this leads to a remarkable enhancement in the electrical characteristics and subsequently, in the electrical performance of the a-Si:H TFT device, resulting in an increase in the drain current from I_{DS} = 1.78x10^{-6} A to 1.71 x 10^{-3} A.

The output characteristics of a-Si:H TFT, at V_{DS} = 2 V, for different gate dielectric materials reveal that as the dielectric constant (k) increases from 3.9 to 300, several effects can be observed:

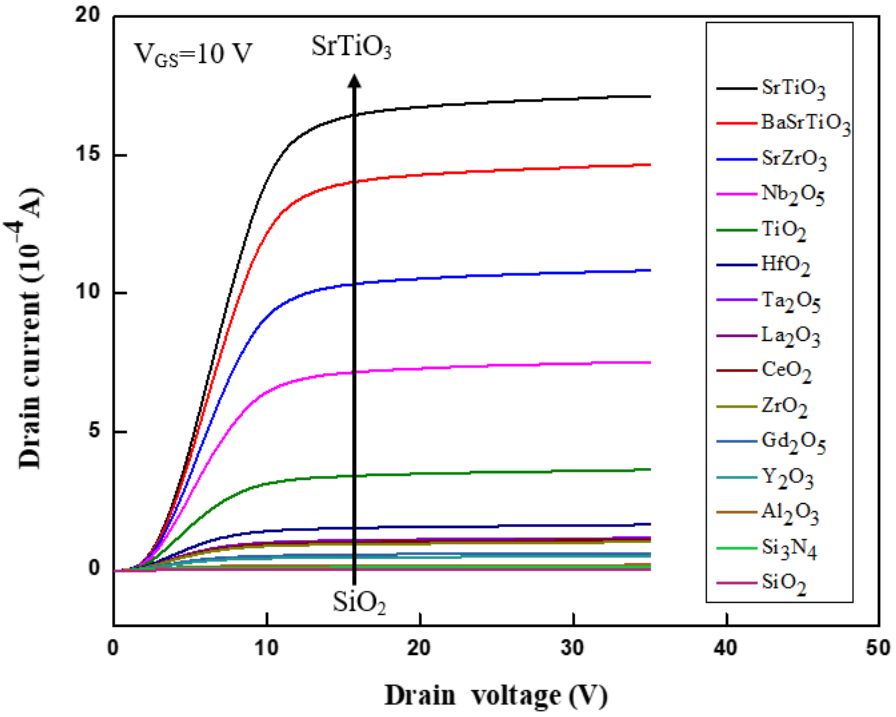

Figure III.5. *Output characteristics of a-Si:H TFT, at V_{GS} = 10 V, for different gate dielectric materials.*

- ✓ ***Increased Drain Current*** : As the dielectric constant increases, the drain current of the a-Si:H TFT shows a significant increase from I_{DS} =1.78x10^{-6} A to 1.71x10^{-3} A. This suggests that a higher dielectric constant enhances the conductivity and current flow in the device.
- ✓ ***Improved Electrical Characteristics***: The increase in dielectric constant leads to a notable enhancement in the electrical characteristics of the a-Si:H TFT. This enhancement can be attributed to the reduction in the electrical thickness of the gate dielectric (Figure III.6), resulting in improved gate capacitance per unit area.

It is important to note that these observations are specific to the mentioned conditions (V_{DS} = 2 V) and the investigated gate dielectric materials. Other factors, such as material properties, device dimensions, and operating conditions, can also influence the output characteristics and performance of a-Si:H TFTs with different gate dielectric materials.

The increase in current in a-Si:H TFT (Thin-Film Transistor) with the increase of dielectric materials can be explained by several factors:

- ✓ The dielectric materials used as gate insulators typically have a higher dielectric constant (**κ**) compared to traditional SiO_2. This higher dielectric constant allows for a higher gate capacitance, which increases the efficiency of the transistor in controlling the flow of current. As a result, more current can flow through the channel region of the TFT.
- ✓ The use of dielectric materials with a higher κ value helps to reduce the effective thickness of the gate dielectric, also known as the Equivalent Oxide Thickness (EOT) (Figure III.6). A thinner gate dielectric results in a higher electric field across the channel region, facilitating the transport of charge carriers and leading to an increase in current.
- ✓ Moreover, the presence of high-k dielectric materials can also minimize the occurrence of quantum tunneling, which is a phenomenon where electrons can tunnel through thin barriers. By reducing quantum tunneling, the leakage current is reduced, allowing for a higher current to be sustained in the device.

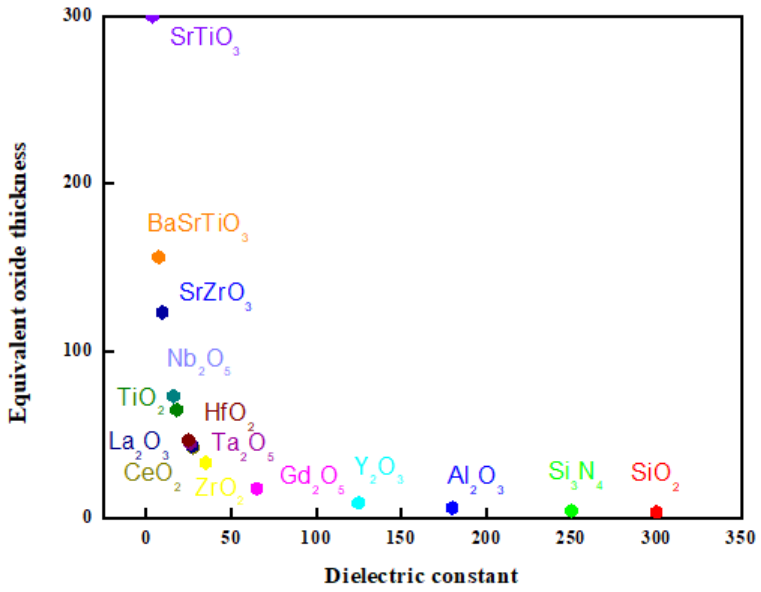

Figure III.6. *Evolutions of equivalent Oxide Thicknessof a-Si:H TFT, depending on the dielectric constant*

Hence, the increase in current in a-Si:H TFT with the increase of dielectric materials can be attributed to the higher gate capacitance, reduced effective thickness of the gate dielectric, and suppression of quantum tunneling, all of which enhance the device's electrical characteristics and performance.

III.3.2.2 Quantification of the phenomenon

Figure III.7.a shows the variation of I_{DS} plots for drain voltages V_{DS} = 2 Volts and for gate voltages V_{GS} = 20 Volts under the effect of the gate dielectric constan. Where we can see that I_{DS} decreases with decreasing κ according to the following equation which extracted using the fitting:

$$I_{DS}(\kappa) = 2{,}62.10^{-5} - 2{,}33\,.10^{-5}\exp(-0{,}019.\kappa) \qquad \text{(III.9)}$$

Figure III.7.b shows the variation of I_{DS} plots for drain voltages V_{DS} = 20Volts and for gate voltages V_{GS} = 10Volts, using deferent κ. Where it can see that I_{DS} is expressly proportional to the gate dielectric constant according to the following equation which extracted using the fitting:

$$I_{DS}(\kappa) = 5{,}83.10^{-6} - 3{,}69\,.10^{-5}.\kappa \qquad \text{(III.10)}$$

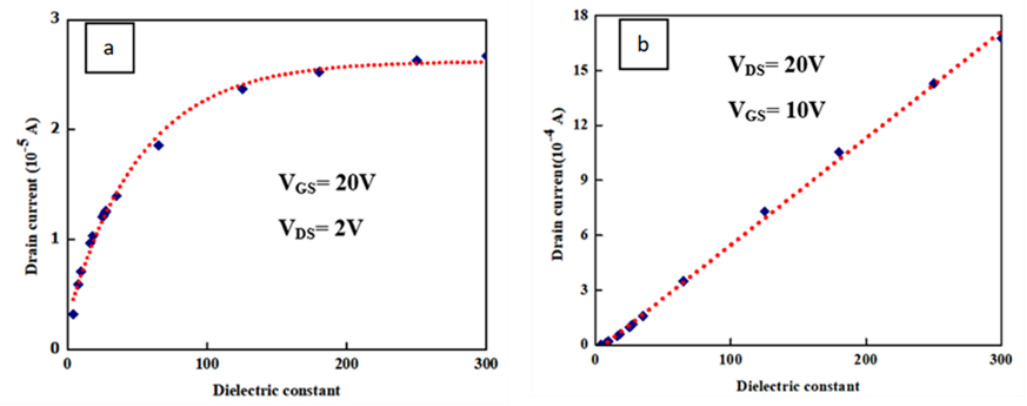

Figure III.7. *Variation of I_{DS} plots using deferent gate dielectric constant for: (a) V_{DS} = 2Volts and V_{GS} = 20 Volts,and (b)V_{DS} = 20Volts and V_{GS} = 10Volts*

The performance parameters using deferent gate dielectric materials extracted from the corresponding transfer characteristics (I_{DS}-V_{GS}) curve are listed in Table III.4.

Table III.4. *Variations of C_i , V_T, μ_{FE}, I_{on}, I_{off}, I_{on}/I_{off}, and SS, respectively, depending on κ*

Dielectric Material	κ	C_i ($\times 10^{-8}$F cm^{-2})	V_T (V)	μ_{FE} (cm^2 V^{-1} s^{-1})	I_{on} (A)	I_{off} (A)	I_{on}/I_{off}	SS (V dec^{-1})
SiO_2	3.9	1.15	6.755	0.104	6.63×10^{-6}	3.24×10^{-11}	2.04×10^{5}	0.85
Si_3N_4	7.5	2.21	4.86	0.0986	1.021×10^{-5}	1.29×10^{-11}	7.91×10^{5}	0.47
l_2O_3	9.5	2.80	4.524	0.0971	1.16×10^{-5}	9.52×10^{-12}	1.22×10^{6}	0.38
Y2O3	16	4.72	4.205	0.0923	1.45×10^{-5}	4.45×10^{-12}	3.25×10^{6}	0.26
d_2O_5	18	5.31	4.09	0.0903	1.52×10^{-5}	3.65×10^{-12}	4.16×10^{6}	0.24
ZrO_2	25	7.37	3.803	0.0862	1.71×10^{-5}	2.40×10^{-12}	7.12×10^{6}	0.2 0
CeO_2	26	7.67	3.771	0.0860	1.73×10^{-5}	2.33×10^{-12}	7.42×10^{6}	0.194
La_2O_3	27	7.96	3.743	0.0854	1.76×10^{-5}	2.28×10^{-12}	7.71×10^{6}	0.190
Ta_2O_5	27.5	8.11	3.72	0.0848	1.77×10^{-5}	2.25×10^{-12}	7.86×10^{6}	0.1889
HfO_2	35	10.32	3.56	0.0813	1.91×10^{-5}	2.00×10^{-12}	9.55×10^{6}	0.1672
TiO_2	65	19.17	3.26	0.0711	2.31×10^{-5}	1.63×10^{-12}	1.41×10^{7}	0.1241
b_2O_5	90	36.87	3.16	0.0469	2.53×10^{-5}	1.50×10^{-12}	1.68×10^{7}	0.1135
$rZrO_3$	180	53.10	3.02	0.0529	3.06×10^{-5}	1.30×10^{-12}	2.35×10^{7}	0.093
$BaSrTiO_3$	250	73.75	2.98	0.0469	3.34×10^{-5}	1.22×10^{-12}	2.73×10^{7}	0.091
$SrTiO_3$	300	88.5	2.96	0.0437	3.50×10^{-5}	1.18×10^{-12}	2.96×10^{7}	0.0891

Figure III.8 regroups the principal performance parameters, including the capacitance per unit area, threshold voltage, field-effect mobility (μ_{FE}), and I_{on}/I_{off} ratio, plotted against the gate dielectric constant (K). It can be seen that as the dielectric constant increases from 3.9 to 300, the foolowing observations can be made:

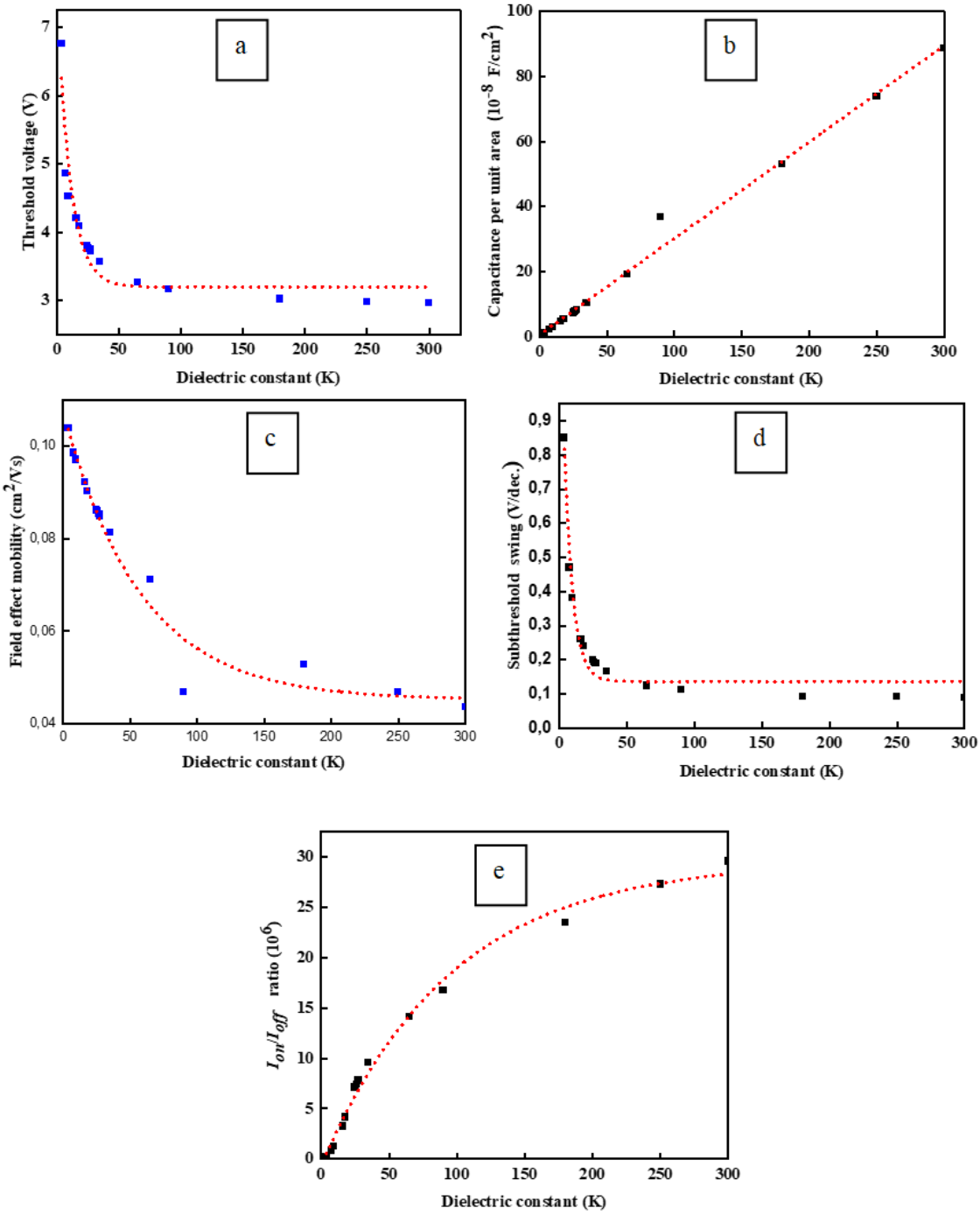

Figure III.8. *Effects of dielectric constant on: (a) threshold voltages, (b) capacitance per unit area, (c) field effect mobility, (d) subthreshold swing and (e) I_{on}/I_{off} ratio*

- ✓ The threshold voltage (Figure III.8.a) decreases from V_T = 6.75 V to V_T = 2.96 V, this can be attributed to the substantial rise in current resulting from the heightened capacitive injection of free charge carriers, specifically electrons; it follows an exponential variation (….) with gate dielectric constant of the form:

$$V_T=3.19579+4.40195\exp(-0.09395\ \kappa) \quad \text{(III.11)}$$

- ✓ The capacitance per unit area (Figure III.8.b) increases from the value $C_i = 1.15 \times 10^{-8}$ F cm^{-2} to the value $C_i = 8.85 \times 10^{-9}$ F cm^{-2}, due to the increase in the dielectric constant for the dielectric material; it follows a variation (….) with κ of the form:

$$C_i = 0.2965+0.57787\ \kappa \quad \text{(III.12)}$$

- ✓ The field-effect mobility (Figure III.8.c) decreases from the value μ_{FE} = 0.104V cm^2 V^{-1} s $^{-1}$ to μ_{FE} = 0.0437 cm^2 V^{-1} s $^{-1}$, this phenomenon arises due to the increase in the capacitance per unit area caused by the reduction in the dielectric constant of the dielectric material, it follows an exponential variation (….) with κ of the form:

$$\mu_{FE}=0.04517-0.06254\exp(-0.01729\ \kappa) \quad \text{(III.13)}$$

- ✓ The subthreshold swing (Figure III.8.d) decreases from the value *SS* = 0.85V per decade to the value *SS* = 0.089V per decade, and This phenomenon can be attributed to the notable increase in the maximum slope of the transfer characteristic in the semi-logarithmic plot, which is a consequence of the substantial increase in the drain current; it follows an exponential variation (….) with gate dielectric constant (K) of the form:

$$SS=0.13669-1.26305\exp(-0.15859\ \kappa) \quad \text{(III.14)}$$

- ✓ I_{on}/I_{off} ratio (Figure III.8.e) increase from the values I_{on}/I_{off} = 2.04 x10^5 , to the values I_{on}/I_{off} = 2.96 x10^7. This is due to the increase in the gate capacitance per unit area; it

follows an exponential variation (….) with gate dielectric constant of the form:

$$I_{on}/I_{off} = 29.64043 + 30.33562 \exp(- 0.01045\ \kappa) \quad \text{(III.15)}$$

Moreover, from a close analysis of the above deduced relations (Eq. III.11 to III.15), it can be concluded that, except the SS linear variation (Eq. III.14), all other investigated TFT electrical parameters, C_i, V_T, μ_{FE}, I_{on}, I_{off}, I_{on}/I_{off} gave a similar exponential dependence of the form:

$$P=P_0+\alpha\exp(\beta d_i) \quad \text{(III.16)}$$

where P_0, α and β are specific constants describing the variation of a given parameter; such constants are summarized in Table III.7. The units indicated refer to their corresponding a-Si:H TFT parameters, whereas α and β are unitless constants. Thus, from these relations, one can straightforward determine the direct determination, for a given a-Si:H TFT of known dielectric thickness, the exact desired parameter (C_i, V_T, μ_{FE}, I_{on}, I_{off}, I_{on}/I_{off}). Moreover, if any of these parameters is determined experimentally, it would then be possible to deduce the exact Si_3N_4 thickness of the investigated a-Si:H TFT.

Table III.5. *Characteristic constant values in the relationship $P=P_0 + \alpha exp(\beta d)$ for all a-Si:H TFT electrical parameters where P represents (C_i, V_T, μ_{FE}, I_{on}, I_{off}, and I_{on}/I_{off}*

Parameter, *P*	**V_T (V)**	**μ_{FE} (cm^2/Vs)**	**I_{on} (10^{-5} A)**	**I_{off} (10^{-11} A)**	**I_{on}/I_{off} ×10^6**
P_0	3.19	0.04	0.93	-0.50	29.64
α	4.40	-0.06	0.99	0.57	30.34
β	-0.094	-0.017	- 0.008	-0.004	-0.010

III.3.3 Electrical Field Distributions

In order to prevent early breakdown in the zones subjected to a strong electric field, it is important to consider the effects of the distribution of electric fields along an electronic device. Two-dimensional distribution of electric field lines in an a-Si:H TFT was

investigated using the Silvaco ATLAS simulator in order to better comprehend the cause of this phenomena.

III.3.3.1 Qualitative observations

Figure III.9 displays the two-dimensional distribution of the electric field lines in the a-Si:H TFT for two distinct gate dielectric materials: (a) SiO_2, (b) ZrO_2, (c) HfO_2, and (d) $SrTiO_3$ at a drain bias, V_{DS}= 2 V and a gate voltage, V_{GS}= 0 V.

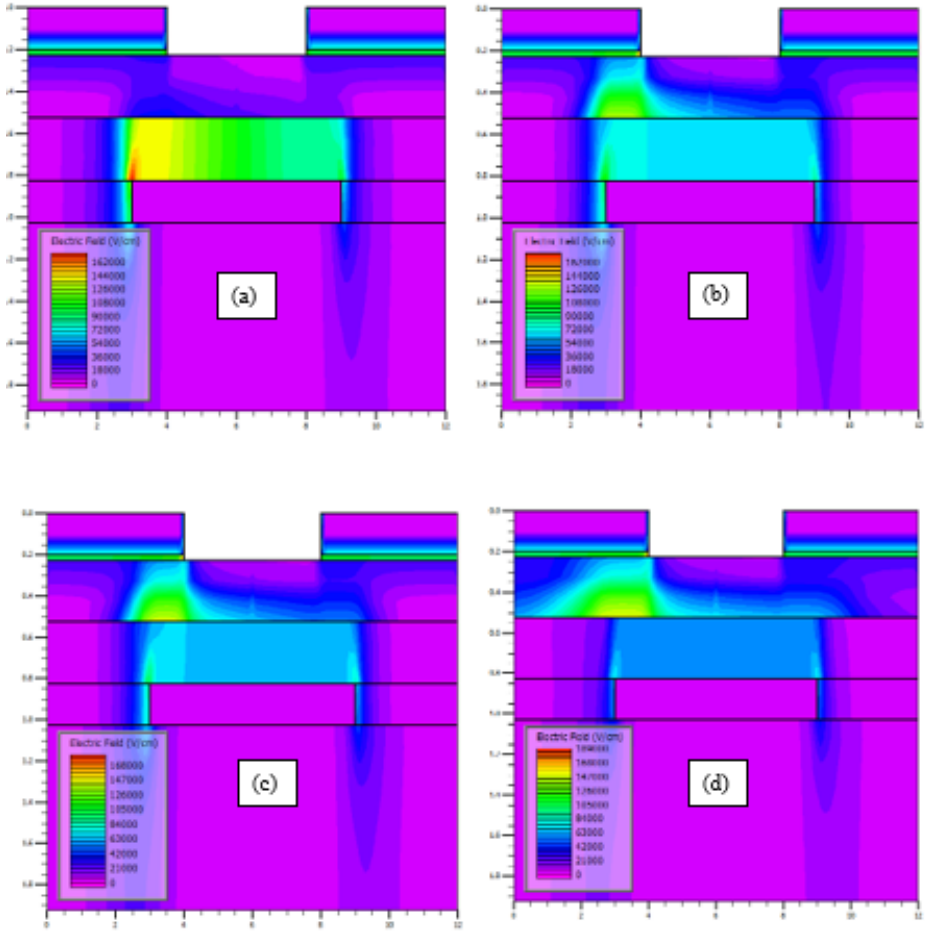

Figure III.9. *2D distribution of the electric field lines in the a-Si:H TFT with gate dielectric materials: (a) SiO_2, (b) ZrO_2, (c) HfO_2, and (d) $SrTiO_3$ at V_{DS}= 2 V and V_{GS}= 0V.*

The obtained results indicate that:

- ✓ There is a dense concentration of electric field lines in the channel region between the gate and the drain.

- ✓ The electric field strength is higher in the channel area near the drain compared to the region close to the source side.
- ✓ The a-Si:H FET with $SrTiO_3$ as the gate dielectric (Figure III.9.b) exhibits a higher density of field lines compared to the structure with SiO_2 as the gate dielectric (Figure III.9.a) under the same conditions.

III.3.3.2 Quantification of the phenomenon

To generalise the above obsedrved phenomena, we considere other dielectric materials ($SrTiO_3$, $BaSrTiO_3$,$SrZrO_3$, Nb_2O_5, TiO_2, HfO_2, Ta_2O_5, La_2O_5, CeO_2, ZrO_2, Gd_2O_5, Y_2O_3, Al_2O_3, Si_3N_4, and SiO_2) as a gate dielectrics; we also extracted the electric field distribution (Figure III.10) along the cutline AA' located at a distance of 0.1 nm from the gate dielectric surface obtained at V_{DS}= 2 V and V_{GS} = 0 V.

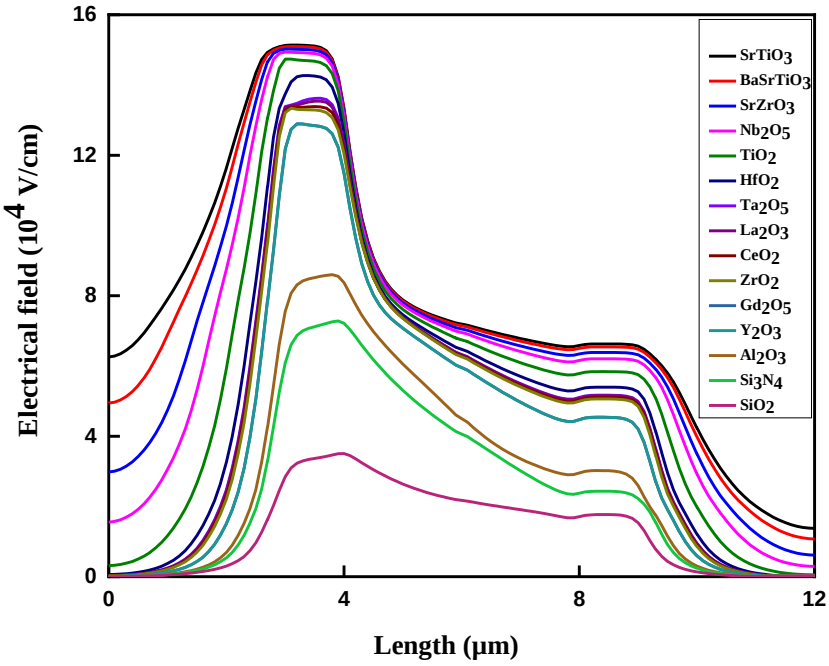

Figure III.10. *Electrical field distribution at AA' cut line by the side of a distance of 0.1 nm from the surface of different gate dielectric materials at V_{DS} = 2 V and V_{GS}= 0 V.*

It is obvious that multiple extremely sharp peaks are formed at the same spot; these peaks signify the maximum achieved electric field as a result of the high voltage at the gate edge next to the drain. To quantify the dependence of maximum achieved electric field by the gate dielectric materials, the maximum peak intensity value of the electric field as a function of the gate dielectric constant in the present a-Si:H TFT, at V_{DS}= 2 V and V_{GS} = 0 V presented in Figure III.11. It can be seen that the curve rises extremely quickly at first (for $\kappa \leq 35$), and subsequently leads to a saturation regime beyond $\kappa > 35$.

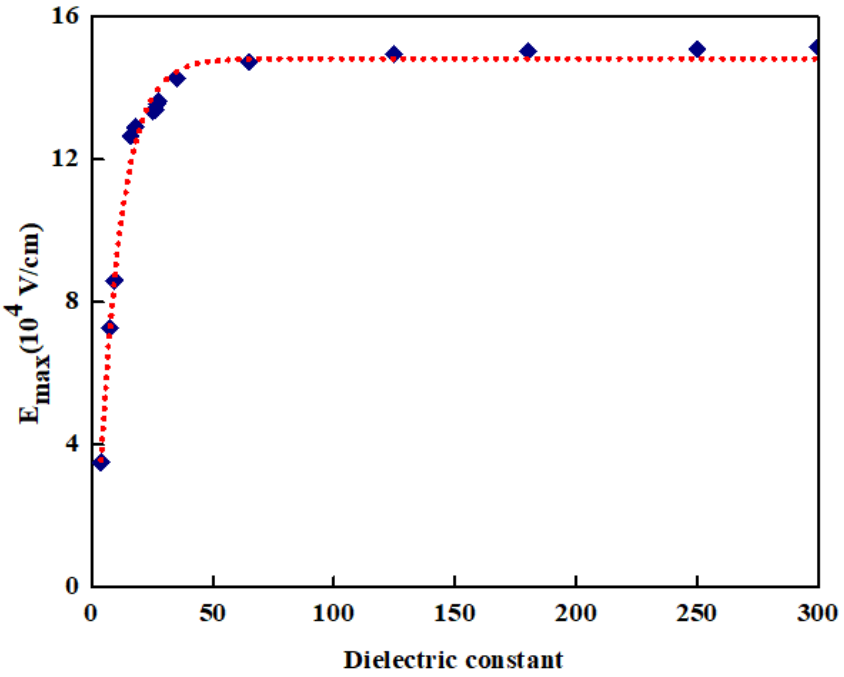

Figure III.11. *Variation of the maximum intensity of electric field in the channel in a-Si:H TFT versus gate dielectric constants, at V_{GS} = 0 V and V_{DS} = 2 V, with curve fitting, dotted-lines (….)*

The quantification of the behaviors of the maximum value of the electric field is carried out through curve fitting, dotted-lines (….) in Figure III.11, it follows an exponential variation (….) with the dielectric constant (K) of the form:

$$E_{max}(10^4 V/cm) = 1{,}48.10^5 - 1{,}73.10^5 \exp(-0{,}11.\kappa) \qquad \text{(III.17)}$$

III.4 EFFECTS OF ACTIVE LAYER THICKNESS

The need for high performance a-Si:H TFTs requires the improvement of their electrical properties via on the optimization of the channel active layer size in particular its thickness. In this context, we carried out numerical simulations using Atlas of Silvaco software highlight the effects of scaling down the a-Si:H active layer thickness, $d_{a\text{-}Si:H}$, on TFT electrical characteristics and parameters. Figure III.12 illustrates the three dimensional (3D) structure of a high-performance bottom-gate a-Si:H TFT, together with the values of its main geometrical constituents.

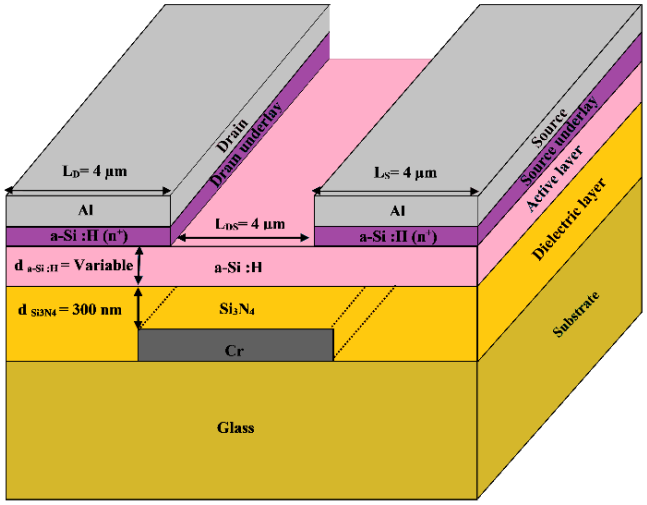

Figure III.12. *3D schematic representation of a bottom-gate a-Si:H TFT structure, with its main geometrical parameters, used for this numerical simulations*

III.4.1 Effects of active layer thickness on DC characteristics

The determination of DC transfer and output characteristics of a thin film transistor is important and essential step for the understanding as well as the improvement of the device's operation and performance.

The (I_{DS} – V_{GS}) transfer characteristics were calculated, in the present work, for different constant V_{DS} values of 2, 10 and 15 V giving similar behaviors. Typical (I_{DS} – V_{GS}) curves are semi-logarithmically plotted, at V_{DS} = 2 V, in Figure III.13 for the presently considered a-Si:H TFT with different a-Si: H active layer thicknesses (varying from 300 down to 15 nm). It is clear that all the transfer curves showed a similar overall behavior for each thickness. In fact, we notice:

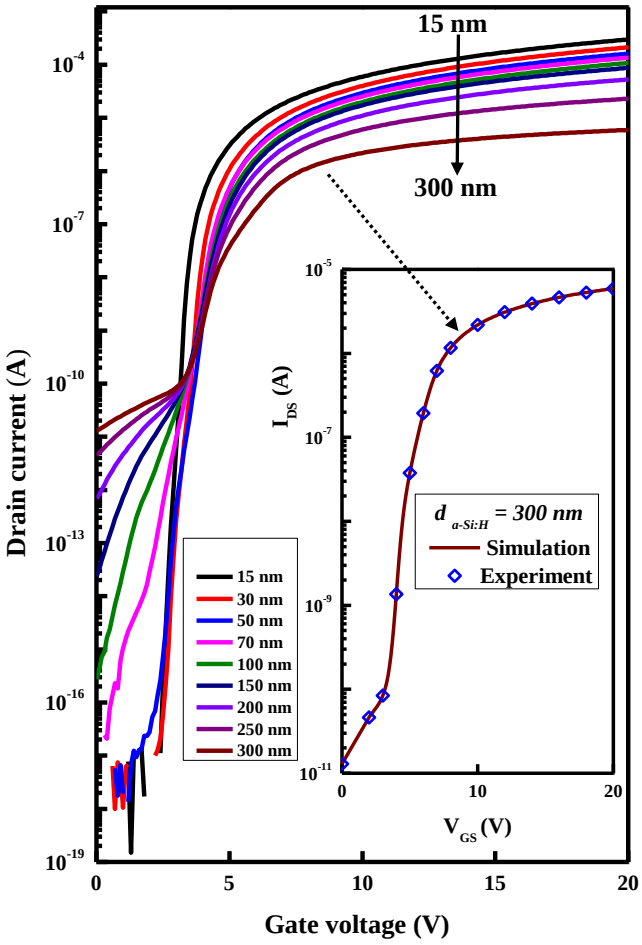

Figure III.13. *Simulated (solid curves) transfer characteristics (I_{DS} – V_{GS}) of a-Si:H TFT calculated at V_{DS} = 2V and different thicknesses of the active layer. The comparison of calculated (——) and experimental data (◊ ◊ ◊)[28], for a 300 nm thick a-Si:H active layer, are shown in the inset*

i. An initial region of low off-current, I_{off}, that generally depends on the properties of the Si_3N_4/a- Si interface and the resistivity of the a-Si film itself [25],

ii. A very sharp increase in I_{DS} due to an electron accumulation layer formed at the Si_3N_4/Si interface [26], and finally,

iii. A quasi-saturation region representing the high on-state current, I_{on}, which is mainly affected by Ohmic contacts, drift mobility, interface states and the gap state density [27].

To put into evidence the validity of the calculated curves, we fitted the unique reported experimental (I_{DS} - V_{DS}) characteristics for an optimized TFT with 300 nm thick a-Si:H active layer [28]. The obtained curve (inset to Figure III.13) showed a good agreement between the simulated curve (——) and that experimentally reported results (◊ ◊ ◊) under the same geometrical and polarization conditions. Thus, putting into evidence the good precision of Silvaco software. The most remarkable and novel observation is the influence of the active layer thickness on transfer characteristics values.

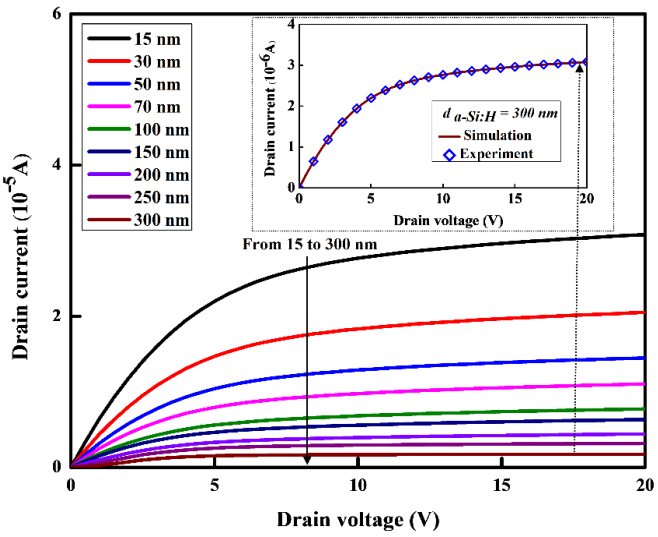

Figure III.14. *Calculated (solid curves) output characteristics (I_{DS} – V_{DS}) of the a-Si: H TFT, calculated at V_{DS} = 10 V and different thicknesses of the active layer. The comparison of calculated and experimental data (◊ ◊ ◊) [28], for a 300 nm thick a-Si:H active layer, are shown in the inset*

The output characteristics of an amorphous silicon Thin-film transistor provide important insights into how the transistor behaves under varying operating conditions and are crucial for optimizing TFT performance. Figure III.14 represents the output characteristics ($I_{DS} - V_{DS}$) for different a-Si:H active layer thicknesses obtained at V_{GS} = 10 V. The comparison between the present simulated and reported experimental results [28], shown in the inset of Figure III.14 for a 300 nm thick active layer, is very good. It can also be seen that, as the drain voltage increases, all curves showed a similar variation trend: they initially increase linearly then saturate for high V_{DS}. However, as the a-Si:H thickness decreases we notice that (i) the saturation of the drain current occurs at higher values and (ii) the slope of the initial variation increases. These observations are quantified below in terms of device parameters.

III.4.2 Quantification of improved device parameters

The observed qualitative effects of scaling down the a-Si:H active layer thickness on TFT parameters (V_T, μ_{FE}, SS, I_{off}, I_{on}, and I_{on}/I_{off} ratio) are analyzed and quantified.

III.4.2.1 Threshold voltage

The threshold voltage is deduced in this work from transfer characteristics via the linear extrapolation method. It should be noted that this parameter can also be determined by different methods such as: match-point, linear extrapolation, second and third-derivative, transition method, normalized mutual integral difference, etc [29,30]. Thus, the obtained results of the effects of the active layer thickness on the threshold voltage are better displayed in Figure III.15. It is clear that as the a-Si:H layer thickness deceases from 300 to 15 nm the threshold decreases from 4.86 V to 1.85 V. This decrease in V_T is attributed to lower currents caused by the capacitive injection of free charge carriers (electrons). In fact, as $d_{a\text{-}Si:H}$ decreases, the capacitance of the layer also decreases, leading to a lower injection of free electrons when a voltage is applied. Thus leading to a lower threshold voltage to achieve the desired switching behavior in the a-Si:H TFT.

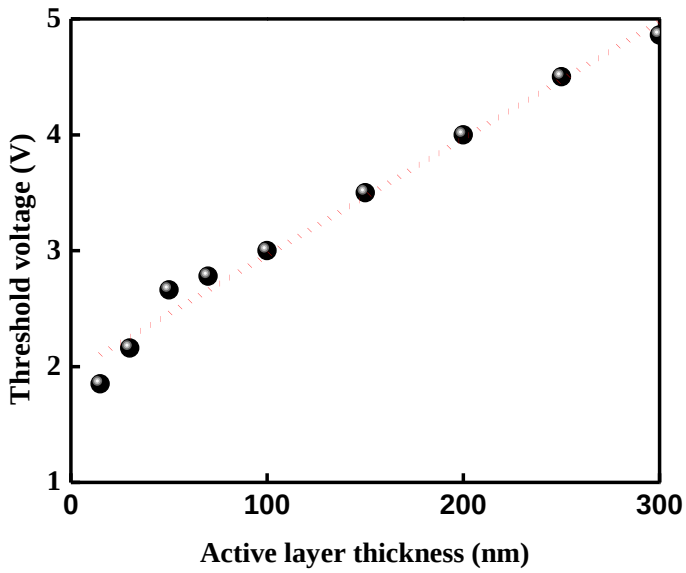

Figure III.15. *Effects of the a-Si: H active layer thicknesses on threshold voltage*

To quantify the effects of the active layer thickness, $d_{a\text{-}Si:H}$, on the threshold voltage, we deduced through curve fitting (**…..**) the following relation:

$$V_T(V) \approx 1{,}95 + 0.01.\, d_{a-Si:H}(nm) \qquad \text{(III.18)}$$

The importance of this relation lies in the fact that one can design such devices with the desired low threshold voltages by just choosing the corresponding active layer thickness. The use of this formula could be extrapolated to even lower thicknesses.

It should be noted that the decrease in V_T values indicates that the voltage level at which a transistor switches from the off-state to the on state occurs at lower voltages. Hence, this situation favors the use of such devices in a matrix of integrated circuits, which requires less applied potentials and consequently less power consumption.

III.4.2.2 Field-effect mobility

The field-effect mobility, a parameter used to describe the electrical behavior of the channel of a transistor, it is given by relation (I.1), recalled below [7, 31-33]:

$$\mu_{FE} = \frac{L_c}{W_c C_i V_{DS}} \left(\frac{\partial I_{DS}}{\partial V_{GS}}\right) \quad \text{(III.19)}$$

Thus, the μ_{FE} values deduced from the above transfer characteristics are plotted in Figure III.16 as a function of the a-Si:H layer thickness. It can be seen that as the thickness decreases from 300 to 15 nm the field-effect mobility increases from 0.10 to 14.55 cm^2/Vs.

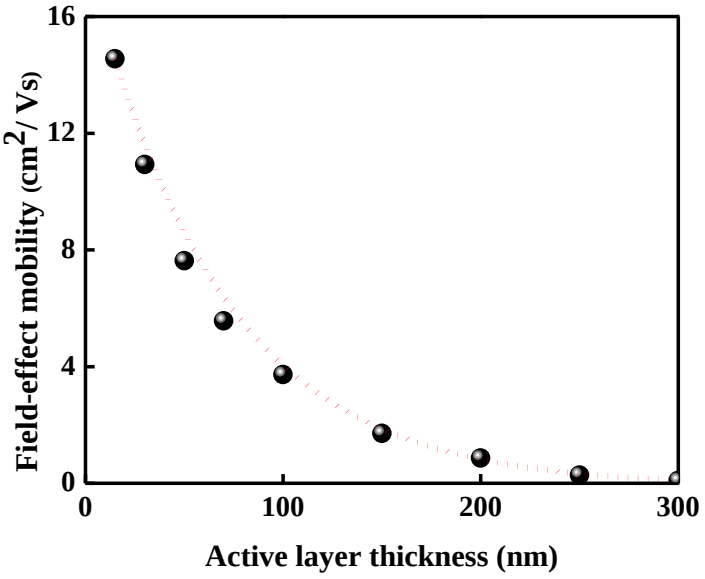

Figure III.16. *Effects of the a-Si: H active layer thicknesses on field-effect mobility.*

For the present a-Si:H active layer, the variation of field-effect mobility is quantified through curve fitting (**.....**) and found to be exponential; it takes the form:

$$\mu_{FE}\left(\frac{cm^2}{Vs}\right) = -0.12 + 18{,}33.\exp[-0.014.\, d_{\text{a-Si:H}}(nm)] \quad \text{(III.20)}$$

Thus, the increase of electron mobility in thinner active layers could be due to fewer defects and trap states and/or carrier confinement that reduces scattering effects. It is worth noting that the increase of mobility is very desirable for faster device applications. In fact, a higher electron motility of the pixel TFTs is very advantageous for improving the performance of very high-resolution displays as well as avoiding the need for external IC mounting of the row and column drivers [34].

III.4.2.3 Subthreshold swing

The obtained results of the subthreshold swing as a function of active layer thickness are plotted in Figure III.17. It can be seen that the scaling down of the active layer thickness from 300 to 15 nm leads to a decrease in the subthreshold swing from 0.47 to 0.04 V/dec. This variation is a result of an increase in the maximum slope of the transfer characteristic resulting from raising the drain current. A lower subthreshold swing for thinner active layers could be due to improved carrier transport, lower trap states, reduced capacitance and enhanced interface quality.

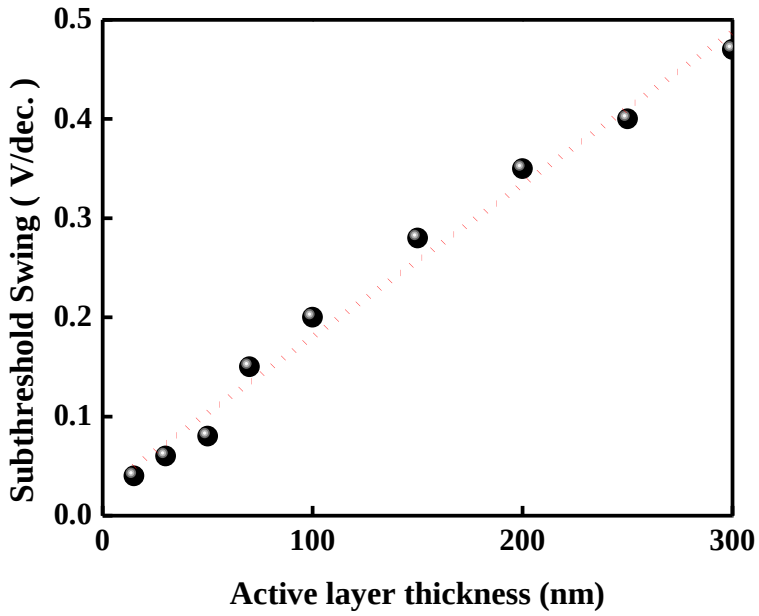

Figure III.17. *Effects of the a-Si:H active layer thicknesses on Subthreshold Swing*

The variation of the subthreshold swing with a-Si:H active layer thickness is quantified through curve fitting; the line of best fit (**…..**) led to the following linear relation:

$$SS(V/dec.) = 0.020 + 0.001 d_{a-Si:H}(nm) \quad \text{(III.21)}$$

The achievement of very low values of *SS* are necessary and needed for the design of devices with fast switching time between the on- and off-states and consequently with less

power consumption. The importance of using this simple formula lies in the design the required devices with desired SS values by choosing the adequate active layer thickness and vice versa.

III.4.2.4 On- and off-state currents

I_{on} and I_{off}, representing the maximum and minimum I_{DS} respectively, are considered to be among the most important parameters in the TFT transfer characteristics. Figure III.18 illustrates the influence of the thickness of a-Si:H active layer on (a) on-state currents, (b) off-state currents and (c) I_{on}/I_{off} ratio.

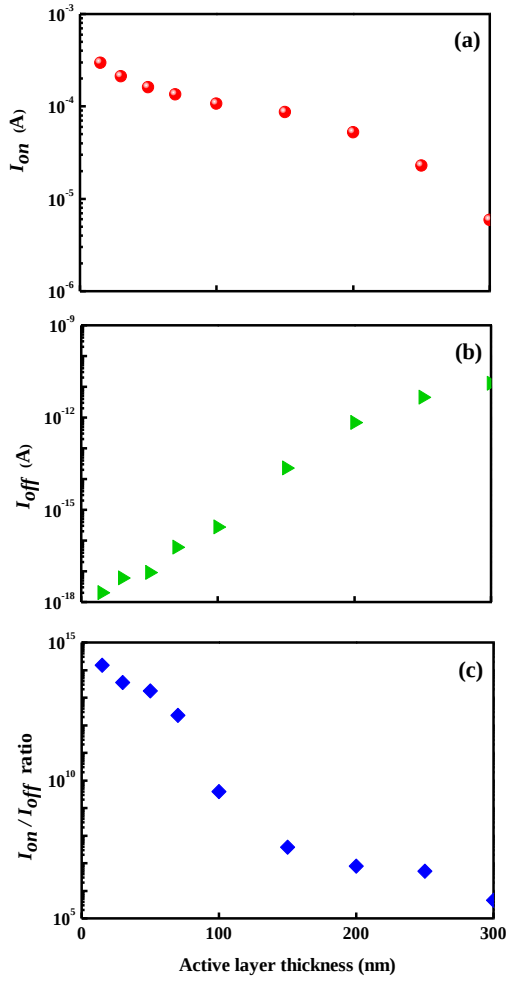

Figure III.18. *Effects of the active layer tthicknesses on: (a) I_{on}, (b) I_{off}, and (c) I_{on}/I_{off} ratio.*

It can be seen that the reduction of $d_{a\text{-}Si:H}$ from 300 to 15 nm leads to (i) an increase of I_{on} from to 5.91×10^{-6} to 2.97×10^{-4} A and (ii) a decrease of I_{off} from to 1.29×10^{-11} to 2×10^{-18} A. The increase of I_{on} with decreasing $d_{a\text{-}Si:H}$ active layer could be attributed to several parameters such as: the improvement of carrier mobility, reduced capacitance, reduced series resistances, etc. The decrease in I_{off} is consistent with the minimization of leakage paths through the active layer and the enhancement of the gate control of the current flow between the source and drain contacts.

Moreover, to evaluate the performance of TFT devices, I_{on}/I_{off} ratio is often used; it characterizes the ratio of the current in the accumulation mode over the current in the depletion mode [3]. This important parameter indicates the ability of the device to switch between on and off states. Figure III.18.c shows the influence of active layer thickness on I_{on}/I_{off} ratio. It can be seen that as active layer thickness ($d_{a\text{-}Si:H}$) decreases from 300 to 15 nm, the I_{on}/I_{off} ratio increases from 4.58×10^{5} to 3.08×10^{14} A; i.e., an enhancement of more than eight orders of magnitude. This large variation is attributed to the simultaneous increase in drain current and the reduction in the off-state.

In conclusion, as the thickness of the amorphous silicon active layer decreased, we noticed from the transfer characteristics a decrease in off-currents, followed by a sharper increase in drain currents and finally an increase in on-currents. Moreover, we also observed, from output characteristics, that the saturation of the drain current occurs at higher values and the slope of the initial variation increases. The analysis and quantification of these observations led to the following conclusions.

The scaling down of the a-Si:H active layer in a TFT from 300 nm to 15 nm showed several interesting variations that are very suitable for specific device applications.

- ✓ Threshold voltage decreased linearly from 4.86 V to 1.85 V. The low voltage level at which a transistor switches from the off-state to the on-state occurs, favors the use of such devices in a matrix of integrated circuits, which requires less applied potentials and consequently less power consumption.

- ✓ Subthreshold swing decreased linearly and from 0.47 to 0.04 V/dec. These very low values of *SS* are necessary and needed for the design of devices with fast switching time.
- ✓ Field-effect mobility increased exponentially from 0.10 to 14.55 cm^2/Vs. This increase in mobility is very advantageous for faster device applications in very high-resolution displays with less external IC mounting of the row and column drivers
- ✓ I_{on} increased from to $5.91x10^{-6}$ to $2.97x10^{-4}$ A and I_{off} decreased from $1.29x10^{-11}$ to $2x10^{-18}$ A, leading to an enhancement of I_{on}/I_{off} ratio of more than eight orders of magnitude.

All the above variations with scaling down the active layer thickness are very much desired for the design of more performing devices to be used in particular applications. Moreover, the importance of the deduced relations between TFT parameters and hydrogenated amorphous silicon active layer, $d_{a\text{-}Si:H}$, lies in the fact that, for any micro- or nano-technological application, one can design such devices with the desired parameters by just choosing the corresponding active layer thickness and vice versa. The use of this formula could also be extrapolated to even lower thicknesses.

III.4 OPTIMALLY IMPOVED A-SI:H STRUCTURE

In order to design an a-Si:H TFT with the most optimal performances, we consder the best optimised parformances obtained with the optimal (i) gate dielectric thickness, (ii) dielectric constant, and (iii) active layer thickness.

III.4.1 Design of the Improved a-Si:H TFT Structure

Figure III.19 illustrates a schematic cross-sectional view Conventional a-Si:H TFT structure, and (b) the improved a-Si:H TFT structure. The improved parameters are indicated on the schematic configuation: gate dielectric thickness = 15 nm, active layer thickness = 15 nm and the dielectric meterial is $SrTiO_3$. The materials and dimensional details of both the conventional [28] and improved a-Si:H TFT structures as specified in Tables III.6. Whereas, Tables III.7 lists the input parameters used for the a-Si:H-based TFT modeling, including the density of states .

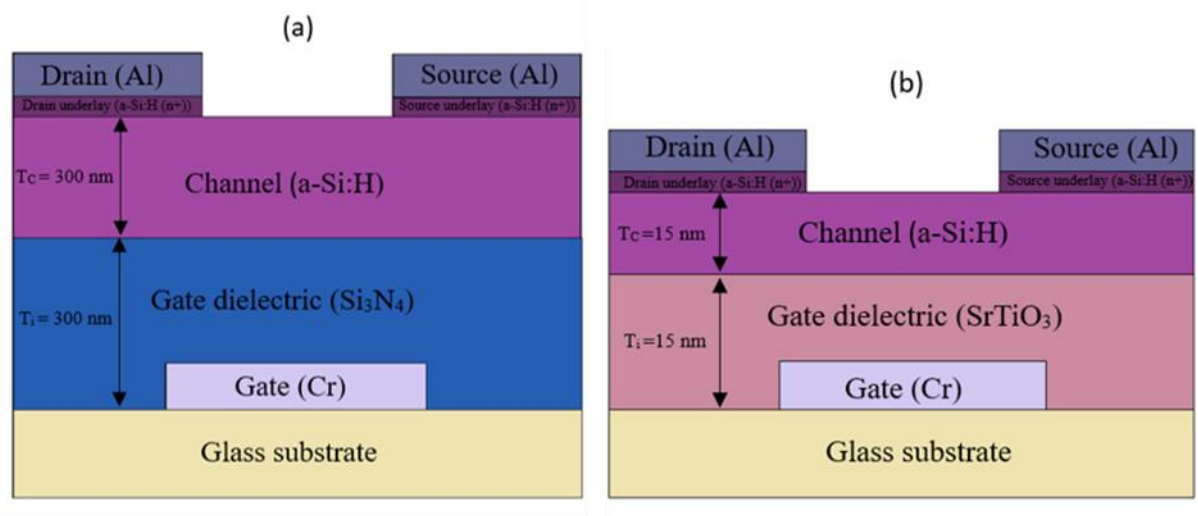

Figure III.19. *Cross section of: (a) Conventional a-Si:H TFT structure, and (b) the improved a-Si:H TFT structure.*

Table III.6. *Dimensions and materials of the Conventional and Optimized a-Si:H TFT structures.*

Parameter	Conventional a-Si:H TFT [28]	Optimized a-Si:H TFT
Channel thickness	300 nm	15 nm
Gate dielectric thickness	300nm	15nm
Gate dielectric material	Si_3N_4	$SrTiO_3$

The source and drain electrodes, made of aluminum (Al), are 200 nm thick and 500 µm wide. These electrodes are deposited over the n^+ a-Si:H regions and slightly overlap the intrinsic channel to enhance carrier injection and collection. Beneath the electrodes, the source and drain extensions consist of n^+-doped hydrogenated amorphous silicon (n^+ a-Si:H), each with a thickness of 25 nm and a length of 4 µm.. The active region, located directly above the gate dielectric layer, is formed by intrinsic hydrogenated amorphous silicon (a-Si:H) with a thickness of 15 nm and a channel length of 12 µm. Serving as the gate dielectric, a 15 nm thick layer of strontium titanate ($SrTiO_3$) ,selected for its high dielectric constant (K), is deposited between the gate electrode and the active layer, maintaining a width of 500 µm. At the base of the structure, a chromium (Cr) gate electrode, 200 nm thick and 500 µm wide, is patterned directly onto the glass substrate, which provides a stable and insulating platform for the entire device architecture.

Table III.7. *Materials parameters of the a-Si:H-based TFT devices structure and DOSs.*

Region	Parameter	Description	Value	Réf.
a-Si:H	*Eg* (eV)	Band gap	1.8	[37]
	□ (eV)	Electronic affinity	3.8	[38]
	ε	Permittivity	11.9	[38]
	C_n (cm^2 V^1 s^1)	Electron capture coefficient	6.4	[39]
	C_P (cm^2 V^1 s^1)	Holes capture coefficient	0.32	[39]
	N_{TA} ($10^{20}cm^{-3}eV^{-1}$)	Density of acceptor-like states at Ec	3.10^{21}	[40]
	N_{TD} ($10^{20}cm^{-3}eV^{-1}$)	Density of donor-like states at EV	3.10^{21}	[40]
	W_{TA} (10^{-2} eV)	Characteristic decay energy of the CBT	0.04	[40]
	WTD (10^{-2} eV)	Characteristic decay energy of the VBT	0.053	[40]
	N_{GA} ($cm^{-3}eV^{-1}$)	Maximum density of the shallow acceptor-like Gaussian states	5.10^{18}	[40]
	N_{GD} ($cm^{-3}eV^{-1}$)	Maximum density of the shallow donor-like Gaussian states	5.10^{18}	[40]
	W_{GA} (eV)	Characteristic deviation of the shallow acceptor-like Gaussian States	0.153	[40]
	W_{GD} (eV)	Characteristic deviation of the shallow donor-like Gaussian States	0.153	[40]
	E_{GA} (eV)	Energy that corresponds to the maximum density of the shallow acceptor-like Gaussian states	0.65	[40]
	E_{GD} (eV)	Energy that corresponds to the maximum density of the shallow donor-like Gaussian states	0.83	[40]
	μ_n ($cm^2V^{-1}s^{-1}$)	Low-field electron mobility	20	[41]
	μ_p ($cm^2V^{-1}s^{-1}$)	Low-field hole mobility	0.12	[41]
	N_C (10^{20} cm^{-3})	Conduction band density at 300 K	2.5	[41,3]
	N_V (10^{20} cm^{-3})	Valence band density at 300 K	2.5	[41,3]
	σ_{TAE} (cm^2)	Capture cross section for electrons in CBT	$2.0x10^{-14}$	[42]
	σ_{TAH} (cm^2)	Capture cross section for holes in CBT	2.5×10^{-15}	[42]
	σ_{TDE} (cm^2)	Capture cross section for electrons in VBT	$2.5x10^{-14}$	[42]
	σ_{TDH} (cm^2)	Capture cross section for holes in VBT	$2.0x10^{-14}$	[42]
Si_3N_4	*Eg* (eV)	Band gap	5	[41]
	k_{Si3N4}	Relative permittivity	7.5	[41,4]
	□ (eV)	Electronic affinity	1.5	[44]
SrTiO3	*Eg*(eV)	Band gap	3.27	[41]
	k_{SrTiO3}	Relative permittivity	300	[41,4]
	□ (eV)	Electronic affinity	4.3	[46]

III.4.2 Device characteristics

he transfer characteristics of both the conventional and optimized a-Si:H TFTs are shown in Figure III.20 in termes of the semi-logarithmic plot of drain current (I_{DS}) versus gate-source voltage (V_{GS}) within the 0 – 20 V range, at a drain-source voltage of V_{DS} = 2 V. This direct comparison between both structures clearly shows substantial enhancements in device characteristics.

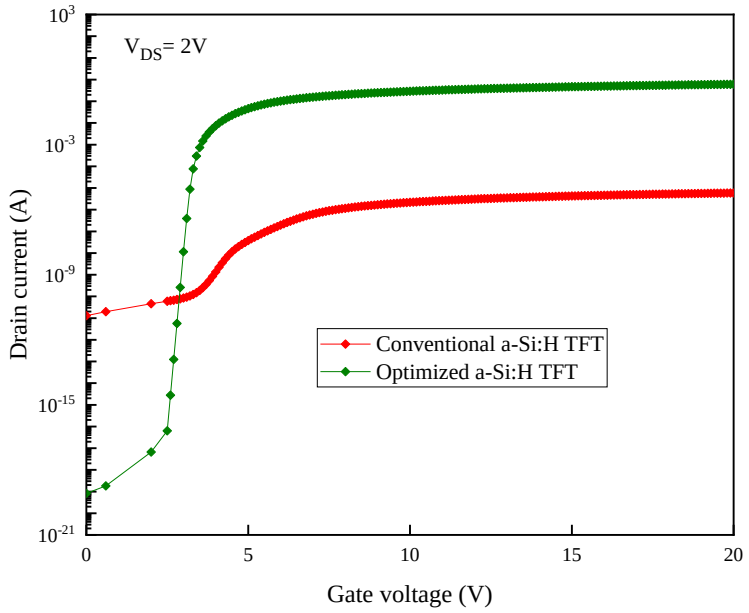

Figure III.20. *Transfer Characteristics of Conventional (-♦-) and Optimized (-♦-) a-Si:H TFT Structures at V_{DS} = 2V.*

The optimized device, (green curve -♦-), displays a distinct advantage in its switching characteristics. A sharp transition from the off-state to the on-state is observed, indicating a well-defined threshold voltage and improved gate control over the channel. Such sharp switching is indicative of stronger electrostatic coupling and lower defect density at the dielectric/semiconductor interface.

In terms of leakage performance, the optimized structure achieves an ultra-low off-state current, dropping below 8.28×10^{-20} A. This outstanding suppression of leakage pathways

demonstrates excellent insulation properties and efficient isolation of the active channel when the device is off. Simultaneously, the on-state current peaks at approximately 0.609 A, reflecting enhanced carrier mobility and efficient charge transport across the channel, likely due to improved film quality and reduced interface traps. As a result, the optimized TFT delivers a very high on/off current ratio, essential for digital switching and low-power electronics. These improvements underline the impact of structural optimization on achieving superior electrical performance.

On the other hand, the conventional structure (red curve -♦-) suffers from several performance limitations. Its off-state current remains significantly higher, around 1.29×10^{-11} A, suggesting ineffective gate modulation and the presence of leakage paths. The on-state current, reaching only about 1.021×10^{-5} A, points to inefficient carrier transport, potentially due to higher trap densities, poor material quality, and increased contact resistance. Consequently, the conventional device exhibits a much lower on/off ratio, making it less suitable for demanding electronic applications.

Hence, these results clearly demonstrate that the optimized a-Si:H TFT structure substantially improves electrical characteristics by minimizing leakage currents, boosting on-state performance, and achieving sharper switching behavior, all critical factors for next-generation thin-film electronic devices.

Figure III.21. shows the output behavior of both conventional (-●-) and optimized (-●-) a-Si:H TFTs, recorded at a fixed gate voltage of I_{GS}= 10 V in over a range from 0 to 20 V. A very noticible contrast between both devices is obtained. The optimized a-Si:H TFT demonstrates a high increase in drain current with increasing V_{DS}, exhibiting rapid growth in the linear region and clear current saturation at approximately 1.08 A. This strong response reflects effective gate control and superior charge carrier transport within the optimized channel. On the other hand, the conventional structure displays poor output characteristics, with a maximum drain current around 1.6×10^{-3} A and a relatively flat curve, indicating suboptimal conduction and weak transistor action. The enlargement of the output caharcteristisc of the conventional device is inserted in Figure III.21.

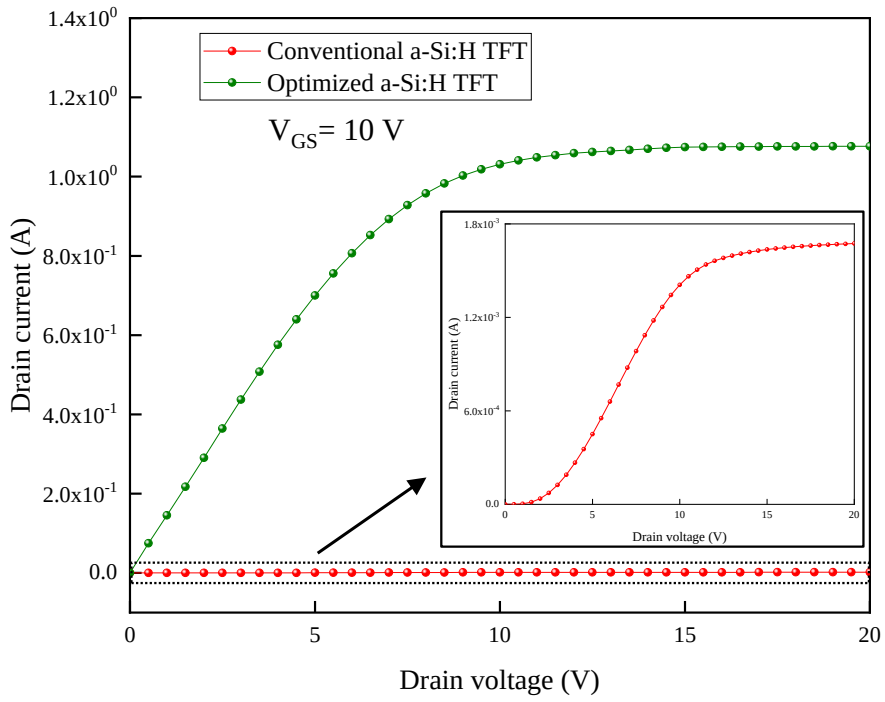

Figure III.21. *Output Characteristics of Conventional (-●-) and Optimized (-●-) a-Si:H TFT Structures at V_{GS} = 10V.*

The enhancements seen in the optimized device arise from the otpimised design improvements, including a thinner active layer, a thicker and higher-quality dielectric, and refined material interfaces. These advancements reduce defect densities, improve carrier mobility, and enhance the electrostatic gate control necessary for efficient device operation. Furthermore, the modifications contribute to lowering leakage currents and promoting a more distinct saturation region at higher drain biases.

III.4.3 Performance parameters

A complete comparison between the conventional and improved a-Si:H TFT structures is presented in Table III.8, revealing high improvements in optimised device performances. Insights drawn from Figure III.20 further confirm the superior electrical behavior achieved.

Table III.8. *Performance parameters of conventional (-♦-) and improved (-♦-) a-Si:H TFT.*

Performance parameters	Symbols	Units	Non-Improved Structures	Improved Structures
Threshold voltage	V_T	V	4.86	3.21
Capacitance per unit area	C_i	F cm^{-2}	2.21×10^{-8}	1.77×10^{-5}
Subthreshold swing	*SS*	V dec^{-1}	0.47	0.02
On-state currents	I_{on}	A	$1.021\text{x}10^{-5}$	0.609
Off-state currents	I_{off}	A	$1.29\ \text{x}10^{-11}$	8.28×10^{-20}
I_{on}/I_{off} ratio	I_{on}/I_{off}	/	$7.91\ \text{x}10^{5}$	7.36×10^{18}

Starting with the threshold voltage (V_T), the improved device shows a notable decrease from 4.86 V to 3.21 V. This shift means the transistor requires less gate bias to switch on, which not only enhances electrostatic control but also leads to reduced power consumption, a key advantage for energy-efficient electronics. Capacitive behavior at the gate interface also benefits from the modifications. The capacitance per unit area (C_i) climbs significantly, from 2.21×10^{-8} F/cm² to 1.77×10^{-5} F/cm², suggesting a much stronger gate coupling effect. This improvement likely results from better dielectric properties and optimized interface engineering. Switching performance, measured by the subthreshold swing (SS), improves impressively as well. The SS drops from 0.47 V/dec in the conventional structure to an outstanding 0.02 V/dec in the improved one. A smaller SS translates to faster and more efficient switching behavior, with less voltage needed to shift the current by an order of magnitude, indicative of fewer interface traps and superior channel control.

Examining the current metrics, the on-state current (I_{on}) in the optimized structure surges to 0.609341 A, a remarkable leap from just 1.021×10^{-5} A in the conventional counterpart. This considerable boost points to enhanced carrier mobility and better channel conductivity under operational conditions. On the other end, leakage current (I_{off}) experiences a dramatic suppression, falling from 1.29×10^{-11} A down to an exceptionally low 8.28×10^{-20} A. Lower leakage currents are essential for low-power applications and indicate excellent insulation quality and minimized parasitic conduction. Crowning the improvements, the Ion/Ioff ratio skyrockets from 7.91×10^{5} to an extraordinary 7.36×10^{18}, signaling unparalleled switching

efficiency. Such a vast difference underscores the successful refinement of the device design, making the improved a-Si:H TFT a highly promising candidate for advanced, high-performance thin-film electronics.

III.4.4 Electrical Field Distributions

Figure III.22 depicts the distribution of electric field lines within the channel of a-Si:H TFTs under the conditions of a gate-source voltage (V_{GS}) of 20 V and a drain-source voltage (V_{DS}) of 2 V, for conventional (Figure III.22.a) and improved (Figure III.22.b) structures.

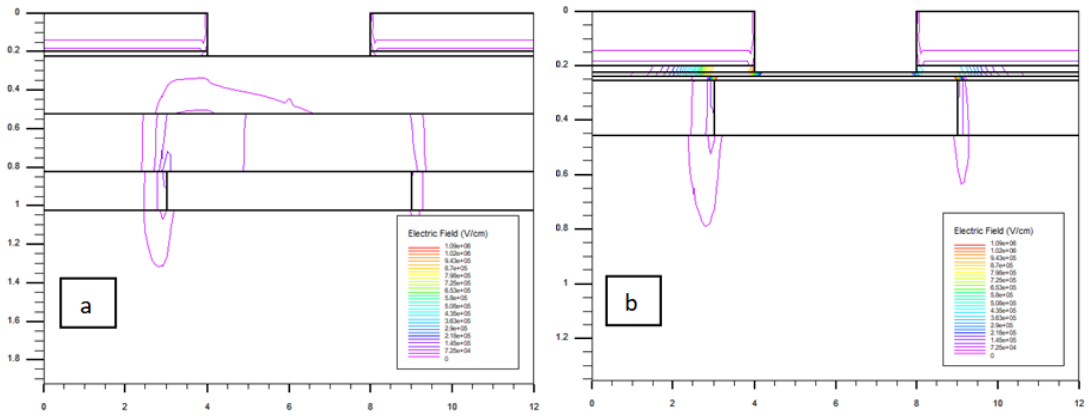

Figure III.22. *Two-dimensional distribution of the electric field lines at V_{GS} = 20V and V_{DS} = 2V for: (a) conventional a-Si:H TFT, and (b) Improved a-Si:H TFT.*

In the conventional a-Si:H TFT, the electric field lines appear dispersed and less concentrated throughout the channel. This indicates weaker electrostatic control, which may hinder the effective formation of the conductive channel, leading to a higher threshold voltage and greater leakage currents. The field lines show a less uniform distribution, especially near the source and drain regions, suggesting inadequate coupling between the gate and the active channel layer.

On the other hand, the improved a-Si:H TFT reveals a more compact and well-defined electric field distribution. The field lines are tightly grouped within the channel, particularly near the interface between the gate and the dielectric. This denser concentration reflects better gate control over the channel, promoting more efficient charge carrier confinement. As a result, the improved structure benefits from higher field-effect mobility, reduced subthreshold swing, and enhanced switching performance. The uniformity in the electric field profile further reduces short-channel effects, improving the overall stability and efficiency of the device.

Figure III.23 shows the electric field distribution along the channel surface for both conventional and improved a-Si:H TFTs, measured at a 0.1 nm distance from the gate dielectric, with V_{DS} = 2 V and V_{GS} sweeping to 20 V.

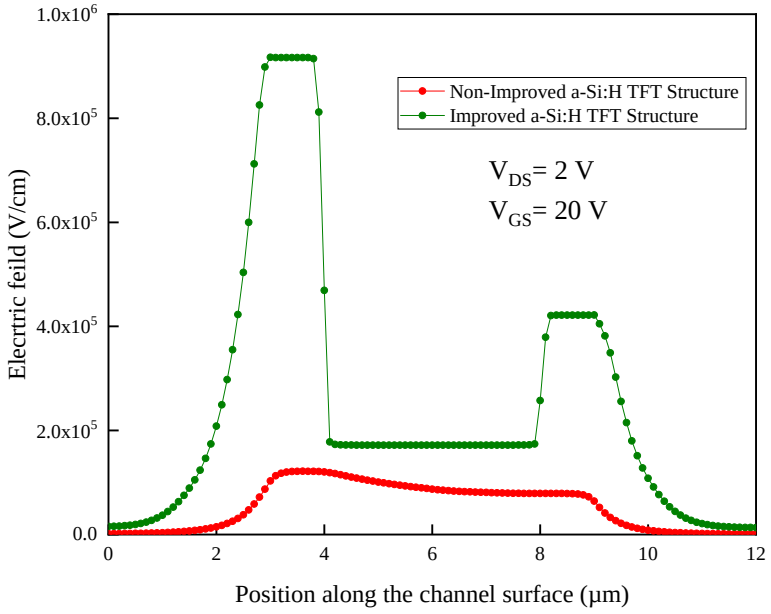

Figure III.23. *Electric field distribution from the left extremity to the right end of the conventional (-●-) and Improved (-●-) a-Si:H TFT Structures.*

The conventional TFT (red curve) shows a low EF, peaking at 1.5×10^5 V/cm, while the improved TFT (green curve) displays a much higher peak at 9.5×10^5 V/cm, almost six times greater. This demonstrates the impact of structural improvements in enhancing charge transport and conductivity.

The improved device's higher electric field suggests better charge accumulation and carrier mobility, likely due to optimized interface layers and reduced trap density. Additionally, it maintains a stable electric field over a broader gate voltage range, unlike the conventional TFT, which shows a decline beyond its peak. This behavior indicates superior electrostatic control and makes the improved a-Si:H TFT more suitable for applications requiring stable, high current performance.

III.5 CONCLUSION

In order to design an a-Si:H TFT with the most optimal performances, we considered three important parameters of this device. (i) gate dielectric thickness, (ii) dielectric constant, and (iii) active layer thickness. To do so, we used SILVACO Atlas simulations to determine the DC current-voltage behavior, including both transfer and output characteristics. From such curves we deduced essential transistor parameters such as threshold voltage, field-effect mobility, subthreshold swing, and on/off current ratio. The effects of thicnkess was taken in range 300 to 15 nm for gate dielctric materials and the a-Si:H active layer. The effects of permitttivity were studiend for many real materials representin high- low-κ dielctrics: $SrTiO_3$, $BaSrTiO_3$,$SrZrO_3$, Nb_2O_5, TiO_2, HfO_2, Ta_2O_5, La_2O_5, CeO_2, ZrO_2, Gd_2O_5, Y_2O_3, Al_2O_3, Si_3N_4, and SiO_2.

Through detailed qualitative and quantitative analyses, it was demonstrated that scaling down the Si_3N_4 dielectric layer thickness from 300 to 15 nm significantly enhance the electric field distribution and improve switching behavior. Similarly, the choice of dielectric material revealed that high-κ dielectrics contributed to stronger gate control, reduced operating voltages, and better device stability compared to low-k counterparts.

Moreover, the study of the effect of active layer thickness showed that its decrease from 300 nm to 15nm led to important improvements in key electrical parameters, including a reduction in threshold voltage, an increase in field-effect mobility, sharper subthreshold swing, and improved current switching capabilities. Thinner active layers enhanced the electrostatic control over the channel and minimized trapping effects.

Finally, the design of an improved a-Si:H TFT structure with the most optimised performance was proposed. It consists of a gate dielectric thickness = 15 nm, and active layer thickness = 15 nm and the dielectric meterial is $SrTiO_3$. This optimized structure demonstrated a clear advancement compared to the conventional design, ensuring better charge transport, faster switching, higher stability, and an overall increase in the reliability and efficiency of a-Si:H TFTs for practical applications, especially in display technologies and sensor systems and opens up new developments of next-generation high-performance electronic devices.

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General Conclusion & Perspectives

Thin-film transistor (TFT) technology based on hydrogenated amorphous silicon (a-Si:H) has become an essential technology for the development of large-area electronic devices, including flat-panel displays and imaging sensors, owing to its attractive advantages such as low fabrication cost, simple process integration, and mechanical flexibility. However, conventional a-Si:H TFT structures still face major challenges related to low carrier mobility, threshold voltage instability, and relatively high subthreshold swing, which limit their performance and reliability in advanced applications.

In this context, in order to design an a-Si:H TFT with the most optimal performances, we considered three important parameters of this device. (i) gate dielectric thickness, (ii) dielectric constant, and (iii) active layer thickness. To do so, we used SILVACO Atlas simulations to determine the DC current-voltage behavior, including both transfer and output characteristics. From such curves we deduced essential transistor parameters such as threshold voltage, field-effect mobility, subthreshold swing, and on/off current ratio. The effects of thicnkess was taken in range 300 to 15 nm for gate dielctric materials and the a-Si:H active layer. The effects of permitttivity were studiend for many real materials representin high- low-κ dielctrics: $SrTiO_3$, $BaSrTiO_3$,$SrZrO_3$, Nb_2O_5, TiO_2, HfO_2, Ta_2O_5, La_2O_5, CeO_2, ZrO_2, Gd_2O_5, Y_2O_3, Al_2O_3, Si_3N_4, and SiO_2.

The major results and conclusions obtained are summarized as follows:

✓ A better control of the electric field distribution across the channel was observed in the proposed structure, leading to a more uniform potential distribution, a reduced peak electric field, and consequently an improvement in threshold voltage stability.

✓ The output characteristics in the saturation regime revealed a significant increase in the drain current, which can be attributed to the enhanced charge carrier transport enabled by the optimized active layer and dielectric interface.

✓ A substantial reduction of the gate-source and gate-drain parasitic capacitances was achieved, thereby improving the switching speed and frequency response of the device.

✓ Field-effect mobility was significantly improved, contributing to faster carrier transport and better drive current capability.

✓ The Ion/Ioff current ratio was enhanced, ensuring lower leakage currents and better device performance in low-power and high-resolution applications.

✓ The subthreshold swing was improved, allowing for sharper switching behavior and lower threshold voltage shifts under prolonged operation.

✓ Furthermore, under high electric field and high-stress conditions, the proposed optimized structure demonstrated more reliable operation compared to the conventional a-Si:H TFT structure.

Finally, the design of an improved a-Si:H TFT structure with the most optimised performance was proposed. It consists of a gate dielectric thickness = 15 nm, and active layer thickness = 15 nm and the dielectric meterial is $SrTiO_3$. This optimized structure demonstrated a clear advancement compared to the conventional design, ensuring better charge transport, faster switching, higher stability, and an overall increase in the reliability and efficiency of a-Si:H TFTs for practical applications, especially in display technologies and sensor systems and opens up new developments of next-generation high-performance electronic devices.

As future perspectives, it would be particularly interesting to fabricate prototypes of this optimized TFT design, based on high-k dielectric integration, using adequate layer deposition techniques. In addition, further research could focus on exploring alternative high-κ materials and multilayer active channel configurations to further enhance the electrical performance and reliability of a-Si:H TFTs, especially for their application in emerging technologies such as flexible electronics, transparent electronics, and next-generation display panel